Fabrication and Characterization of Organic Field-Effect Transistors with Modified Gate Dielectrics and Application for Organic Nonvolatile Memory Cells

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Abbreviations, Constants and Symbols

Abbreviations

2-D	two-dimensional
3-D	three-dimensional
a-Si	amorphous silicon
AFM	atomic force microscopy
Ag	silver
Al	aluminium
Al_2O_3	aluminium oxide
Au	gold
BZT	barium zirconate titanate
CO_2	carbon dioxide
CTL	charge-trapping layer
Cu	copper
CuPc	copper phthalocyanine
CYTOP	poly(perfluoroalkenyl vinyl ether)
D-A	donor-acceptor
DSA	drop shape analyzer

E-beam	electronic beam
EEPROM	electrically erasable programmable read-only memory
F15-NTCDI	N,N′-bis(1H,1H-perfluorooctyl)naphthalene-1,4,5,8-tetracarboxylic diimide
FeFET	ferroelectric field-effect transistor
H_2O	water
HOMO	highest occupied molecular orbital
IEEE	Institute of electrical and electronics engineers
ITO	indium tin oxide
IV	current voltage
LCD	liquid crystal display
LUMO	lowest unoccupied molecular orbital
MEH-PPV	poly[2-methoxy-5-(2-ethyl-hexyloxy)-p-phenylene-vinylene]
Mo	molybdenum
MOSFET	metal-oxide-semiconductor field-effect transistor
MXD6	poly(m-xylylene adipamide)
O_2	oxygen
O_3	ozone
OFET	organic field-effect transistor
OLED	organic light-emitting diode
ONVM	organic nonvolatile memory
OPV	organic photovoltaic
OTS	octadecyltrichlorosilane
OWRK method	Owens,Wendt,Rabel,Kaelble method
PαMS	poly(α-methyl styrene)
P(VDF-TrFE)	poly(vinylidene fluoridetrifluoroethylene)
P/E	program/erase
P3HT	poly(3-hexylthiophene)

P4MS	poly(4-methyl styrene)
PAC	polyacetylene
PBTTT	poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene)
PMMA	poly(methyl methacrylate)
PPV	poly(p-phenylene vinylene)
PQT	polyquaterthiophene
PS	polystyrene
Pt	platinum
PTPTP	1,4-bis(5-phenyl-2-thienyl)benzene
PVA	polyvinyl alcohol
PVD	physical vapor deposition
PVDF	polyvinylidene fluoride
PVN	poly(2-vinyl naphthalene)
PVP	polyvinylpyrrolidone
RAM	random-access memory
RFID	radio frequency identification card
ROM	read-only memory
SAM	self-assembled monolayer
Si	silicon
Si_3N_4	silicon nitride
SiO_2	silicon dioxide
SMU	source/monitor unit
SPM	scanning probe microscopy
Ta_2O_5	tantalum pentoxide
TFT	thin-film transistor
UV	ultraviolet

Constants

ϵ_1	permittivity of PαMS	$2.5 \times 10^{-13}\,\mathrm{A\,s\,V^{-1}\,cm^{-1}}$
ϵ_2	permittivity of SiO_2	$3.4 \times 10^{-13}\,\mathrm{A\,s\,V^{-1}\,cm^{-1}}$
q	elementary charge	$1.6 \times 10^{-19}\,\mathrm{A\,s}$

Symbols (units in square brackets)

ΔV	memory window	[V]
Δ	interface dipole	[eV]
μ	carrier mobility	$[\mathrm{m^2\,V^{-1}\,s^{-1}}]$
μ_e	field-effect mobility	$[\mathrm{m^2\,V^{-1}\,s^{-1}}]$
Φ_{Au}	Au work function	[eV]
ϕ_e	energy barrier for electrons	[eV]
ϕ_h	energy barrier for holes	[eV]
σ_l	surface energy of liquid	$[\mathrm{N\,m^{-1}}]$
σ_s	surface energy of solid	$[\mathrm{N\,m^{-1}}]$
σ_{ls}	interfacial tension between solid and liquid	$[\mathrm{N\,m^{-1}}]$
θ	contact angle	[°]
C_t	total gate capacitance of the transistor	[F]
C_i'	gate dielectric capacitance per unit area	$[\mathrm{F\,m^{-2}}]$
d_e	thickness of electret	[m]
d_{Au}	thickness of gold	[m]
d_c	thickness of charge-trapping layer	[m]
d_{ox}	thickness of silicon dioxide	[m]
d_t	thickness of tunneling layer	[m]
E	electric field	$[\mathrm{V\,m^{-1}}]$
E_e	electric field in electret	$[\mathrm{V\,m^{-1}}]$
E_F	Fermi level	[eV]

$E_{e,max}$	maximal electric field in electret	[V m^{-1}]
E_{e0}	critical electric field in electret for tunneling	[V m^{-1}]
E_{vac}	vacuum electron affinity	[eV]
I_D	drain current	[A]
I_{DS}	drain-source current	[A]
J	current density	[A m^{-2}]
L	channel length	[m]
P	pressure	[Pa]
Q	stored charge	[C]
r_p	deposition rate of pentacene	[Å s^{-1}]
r_{Au}	deposition rate of gold	[Å s^{-1}]
t_P	programming time	[s]
t_{int}	time interval between two read processes	[s]
t_{read}	read time	[s]
t_{RE}	retention time	[s]
v	velocity of the charge carrier	[m s^{-1}]
V_D	potential at drain electrode	[V]
V_G	potential at gate electrode	[V]
V_S	potential at source electrode	[V]
$V_{D,read}$	V_D at read mode	[V]
V_{DS}	drain-source voltage	[V]
V_E	erasing voltage	[V]
$V_{G,read}$	V_G at read mode	[V]
V_{GS}	gate-source voltage	[V]
V_{on}	turn-on voltage	[V]
V_P	programming voltage	[V]
V_{th}	threshold voltage	[V]
W	channel width	[m]

Chapter 1

Introduction

1.1 Overview of Organic Semiconductors

The discovery of conductive polymers, which was rewarded with the 2000 Nobel Prize in chemistry [1], opened the door to a vast world of organic electronics. Compared to inorganic electronics, electronic devices made of organic materials demonstrate unique properties, including mechanical flexibility, light weight, and solution-processable at relatively low temperatures [2]. These properties promise bright prospects in many applications, such as wearable electronics, large-area flexible displays, implantable medical sensors, chemical alarm sensors, etc. Until 2019, the overall market for printed, organic and flexible electronics has become as large as $37.1 billion. This market size is forecast to reach $74 billion in 2030, according to *IDTechEx* [3].

The conductivity of organic semiconductors originates from the molecular conjugation, which often occurs in molecules with alternating single and double covalent bonds between carbon atoms. Conjugation induces delocalized π-electrons that are mobile inside a conjugated molecule and can be transferred among the adjacent molecules by applying an external electric field [4]. In accordance with different molecular forms, organic semiconductors are usually distinguished into conjugated small-molecule materials and conjugated polymers. Conjugated small-molecule organic semiconductors usually have a higher number of benzene rings, such as tetracene, pentacene, rubrene, etc. They can be formed as crystalline or polycrystalline films and have high carrier mobilities up to 20 cm^2/Vs [5, 6]. However, most small-molecule thin films have to be pre-

pared through high-cost vapor deposition techniques due to their insolubility. On the other hand, conjugated polymers are normally composed of repeated units of aromatic cycles or double bonds, such as poly(3-hexylthiophene) (P3HT), polyacetylene (PAC), poly(p-phenylene vinylene) (PPV), etc. They are soluble in common organic solvents, which enables the utilization of low-cost solution-based manufacturing techniques like spin coating, drop coating or inkjet printing. The finished films are amorphous and usually have lower carrier mobilities in comparison with small-molecule materials.

In general, organic semiconductors can be applied in three types of electronic devices: organic field-effect transistors (OFETs), organic light-emitting diodes (OLEDs), and organic photovoltaics (OPVs). Since transistors work as basic elements in many functional circuits, including amplifiers, logic gates, and memories, the study of OFETs has its irreplaceable position.

1.1.1 Organic Transistors

In the 1980s, first OFETs based on conjugated small-molecule materials [7–9] and conjugated polymers [10, 11] were fabricated in succession. The field-effect mobilities of those early OFETs were very low and in the range of 10^{-6} to 10^{-4} cm^2/Vs. In the following decades, the device performance of OFETs has been continually improved by discovering new functional materials and optimizing fabrication technologies [12–21]. Recently, some OFETs have achieved high field-effect mobilities of more than 5 cm^2/Vs already [15].

In particular, the modification of gate dielectrics is one of the most important optimization methods for OFETs. Several early research works [22, 23] have already mentioned the influence of the interface between gate dielectric and semiconductor layer on the electrical parameters of OFETs, such as field-effect mobility and threshold voltage. The reason is that carrier transport depends on the ordering of the semiconductor molecular layers close to the gate dielectric. In order to improve the device performance of OFETs, various methods have been proposed for the modification of the gate dielectric over time, such as creating a self-assembly monolayer (SAM) [24,25], inserting buffer layers [26,27], applying plasma treatment [16], heating [28], illuminating by lights [29,30], etc. Practically, surface modification is supposed to improve the device performance of transistors through simple manufacturing processes.

The development of high-performance OFETs laid the foundation of practical applications of OFETs in novel electronic systems. For example, the company

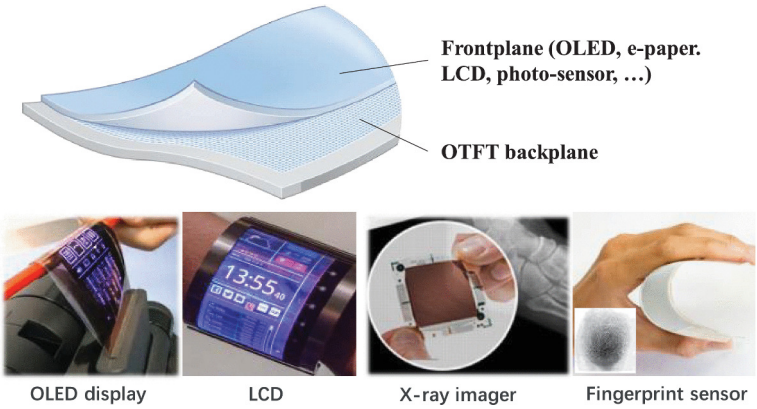


Figure 1.1. Illustration of fully flexible applications based on the organic thin-film transistor (OTFT) backplane technology from *FlexEnable*, reprinted from [31] © 2017 IEEE.

FlexEnable has recently developed a plastic e-paper [31], which contains a full-flexible OLED display integrated with OFET-based switches and current drivers, as shown in Fig. 1.1. The use of flexible OFETs enabled the mechanical flexibility of the display. Besides display array backplanes, OFETs also have high potential to be utilized in other electronic systems, such as RFID cards, electronic labels, chemical sensors, etc.

1.1.2 Organic Nonvolatile Memory Cells

The remarkable progress in OFETs has also driven the development of another important electronic component – organic nonvolatile memory (ONVM), which is responsible for the storage of data in an electronic system. Due to the natural compatibility with the fabrication of OFETs, transistor-based ONVMs have attracted a lot of interest over the last decade. In 2002, Katz *et al.* firstly demonstrated the concept of transistor-based ONVMs with OFETs of different combinations of organic semiconductors (p-channel PTPTP and n-channel F15-NTCDI) and gate dielectrics (SiO_2, glass resin, P4MS, and TOPAS® cyclic olefin copolymer) [32]. In those transistors, they observed a charge storage effect in the gate dielectric by applying a depletion voltage on the gate electrode. The stored charge could be retained for approx. 10 min or for tens of program/erase cycles. This dielectric layer is also called electret, which is defined

as “dielectric materials exhibiting a quasi-permanent electrical charge or dipolar polarization” [33]. Two years later, Unni *et al.* and Schroeder *et al.* reported ONVM devices based on OFETs with ferroelectric dielectrics of poly(vinylidene fluoride-trifluoroethylene) P(VDF-TrFE) [34] and poly(m-xylylene adipamide) (MXD6) [35], respectively. Noticeable nonvolatile memory behavior was found in both devices, including the large ratio between the “ON” and “OFF” currents of more than 200 and the retention time of several hours. Here, the controllable polarization of ferroelectric gate dielectrics gives rise to bistable transfer curves of the transistors, leading to two logic states of the output currents. In the later years, new proposals were basically extensions of the early design ideas, and fabricated devices can be roughly divided into two groups, namely ferroelectric OFETs and charge-trapping OFETs.

Especially, ONVMs based on charge-trapping effects have recently become a hot research topic because of their high device performance. The general understanding that regards the whole electret layer as a trapping layer that stores charges has also been updated by recent research works [36–38]. It is now believed that the electret layer or a part of it, depending on its thickness, actually works as a tunneling layer in a charge-trapping OFET device during programming processes and acts as a blocking layer in retention mode. Accordingly, the design of floating-gate like ONVMs emerged by embedding conductive or semiconductive nanoparticles as trapping centers in electrets of OFET-based ONVMs [39–42]. Optimization methods for this type of devices are usually considered by reducing the thickness of the electret layer or increasing the amount of embedded nanoparticles. However, the implementation of the nanoparticles normally requires complicated manufacturing processes. A recent work from Xu *et al.* [43] has provided an alternative strategy. They utilized an insulating layer with high trapping properties instead of nanoparticles as the storage layer, which avoided complicated processes of inserting nanoparticles into the insulator. The split of an electret into a tunneling layer and a trapping layer, namely a bilayer-electret structure, provides better potential for the fabrication of ONVMs compared to the concept of nanoparticle floating gates.

1.2 Motivation and Aim of the Dissertation

As mentioned above, even though nanoparticle floating-gate ONVMs showed some progress, it is more meaningful to develop ONVM devices that require less

complicated fabrication processes. So far, the development of ONVMs based on charge-trapping OFETs is largely dependent on the selection of suitable materials for the gate stack. Seeking a solution-processable tunneling layer and a charge-trapping layer for the construction of bilayer-electret structures is of high interest. In addition, the storage mechanism, which is very important to guide device optimization, still requires deeper understanding. Hence, this thesis aims to design and fabricate high-performance charge-trapping ONVM cells based on the charge-trapping effects in gate dielectrics, and investigate the physical principles of such ONVM devices. Furthermore, this dissertation also discusses electrical properties of pentacene-based OFETs with surface modification of the gate dielectric, which is an indispensable precondition for the realization of OFET-based ONVM devices.

1.3 Organization of the Dissertation

The dissertation is divided into 7 chapters. Chapter 2 firstly gives a brief but comprehensive overview on the theoretical basics about OFETs, such as materials, structures, and operation mechanisms. Then, the second section of Chapter 2 provides insights into the basic concepts of a nonvolatile memory cell and the typical realization of ONVM cells based on OFETs. Subsequently, Chapter 3 introduces experimental details about fabrication technologies, equipments, measurement platforms, and characterization methods. Following, the influences of gate dielectric surface modification on the electrical properties of OFETs are investigated in Chapter 4. Two modification methods are utilized, namely the insertion of buffer layers and a UV-ozone treatment. In Chapter 5, the fabrication procedure of ONVM transistors is demonstrated, and then the effects of device structural parameters on memory performance are discussed. In Chapter 6, optimization of ONVM devices is carried out by applying thin SiO_2 substrates and a bilayer-electret structure. The memory mechanism of bilayer-electret ONVM devices is also summarized at the end of this chapter. Finally, a summary of this dissertation and outlooks for possible future works are given in Chapter 7.

Chapter 2

Organic Field-Effect Transistors: Materials, Structures, Operation and Application as Nonvolatile Memory Cells

This chapter is divided into two sections. Sec. 2.1 provides an insight into the basics of OFETs, including relevant materials, device geometric structures, operation mechanism, and important electrical parameters. The aim is to give a short but comprehensive introduction for the main research subject of this thesis. In Sec. 2.2, we come to the topic of organic nonvolatile memories. This section starts with several basic concepts of nonvolatile memory cells. Afterwards, three typical approaches of OFET-based ONVMs and their corresponding storage mechanisms are discussed.

2.1 Basics of OFETs

OFET devices are based on the architecture of preexisting thin-film transistors (TFTs), which are normally manufactured with hydrogenated amorphous silicon (a-Si) in industry and applied in large-area electronic systems, such as flat-panel liquid crystal displays (LCD) and imagers [44]. Early organic TFTs, however, suffered from low field-effect mobilities and high threshold voltages, and thus had few practical applications [13]. Many efforts have been made in synthesizing

new materials and optimizing manufacturing techniques over the past decade. Currently, organic transistors can attain comparable carrier mobilities to or even higher than a-Si TFTs [31]. The improved device performance and intrinsic advantages of organic semiconductors, such as solution processability, mechanical flexibility, and stretchability, now attract more and more interest in the area of OFETs.

2.1.1 Materials

An OFET is composed of five functional components: an active layer, an insulating layer, and three electrodes (gate, drain, and source). The natural variety of organic materials contributes to a wide selection range for each specific part, but also increases the difficulty to find materials that balance device performance and manufacturing complexity. In the current status of research on OFETs, it is still a big challenge for the whole community to define a standard material stack. In this subsection, we will have a brief overview of materials pertinent to OFETs. The materials are sorted according to their functions in OFETs.

2.1.1.1 Organic Semiconductors: Active Layers

Organic semiconductors are the basis of charge carrier transport in OFETs. The intrinsic charge carrier mobility of organic semiconductors set the upper limit of the device performance of an OFET. Numerous organic semiconductors were found and applied as transistor materials in the last decades [6,45]. They can be classified into conjugated polymers and small molecules, differentiated by their molecular mass. Some representative materials are listed in Fig. 2.1.

Most conjugated polymers are soluble in common organic solvents, and thus polymeric semiconductor thin films can be easily prepared by solution processes, such as spin coating, drop coating, or inkjet printing. Part of the most studied semiconducting polymer families in this context are alkyl-substituted polythiophenes. The first solution-processed polymer OFET was realized by utilizing a soluble regiorandom poly(3-hexylthiophene) (P3HT) [46], whose field-effect mobility was estimated in the 10^{-4} to 10^{-5} cm^2/Vs range. In later works [47–50], field-effect mobilities of P3HT-based OFETs could be enhanced to the range of 0.01 - 0.1 cm^2/Vs by increasing the degree of head-to-tail regioregularity in P3HT synthesis. However, transistors based on P3HT commonly showed instability in ambient air. Later research works were thus done with the consideration of air

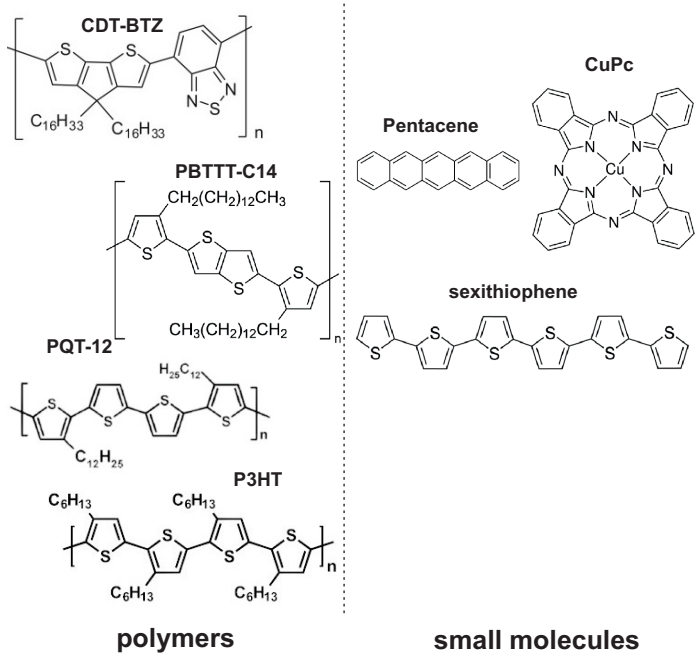


Figure 2.1. Molecular structures of polymeric and small-molecule organic semiconductors that are mentioned in Sec. 2.1.1.1

stability of materials as well [51]. Recently, novel conjugated polymers, such as region-regular polyquaterthiophenes (PQTs) [52], poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene) (PBTTT) [53], and donor-acceptor (D-A) copolymers [21,54], have not only higher carrier mobilities (some of them even surpass the value of 1 cm^2/Vs), but also stable properties in ambient air.

In contrast to polymers, small molecular organic semiconductors are usually formed as films with polycrystalline or crystalline structures via thermal evaporation processes. Widely studied materials include sexithiophene, copper phthalocyanine (CuPc), and pentacene. Among them, pentacene has been intensively researched and provides one of the highest carrier mobilities among the emerging organic semiconductors. Pioneer works based on pentacene were done by Lin *et al.* in the late 1990s [22, 23, 55]. Their fabricated OFETs achieved high field-effect mobilities of more than 1 cm^2/Vs. Over the following years, field-effect mobilities of pentacene-based OFETs have been further improved. For example, Choi *et al.* [56] reported an OFET made of a polycrystalline film of pentacene with a field-effect mobility as high as 6 cm^2/Vs, and Jurchescu *et al.* [57] reported an OFET device made of carefully prepared single crystals of pentacene with a field-effect mobility that exceeds 30 cm^2/Vs. These works reveal superior properties of pentacene for basic theoretical research, including stable and high electrical performance, precisely controllable manufacturing processes, and extensive application in the community. Hence, pentacene is also chosen as the organic semiconductor material for the investigation on OFETs and OFET-based ONVMs in this thesis.

2.1.1.2 Gate Dielectrics: Insulating Layers

In an OFET, a gate dielectric insulates its gate electrode from the active layer and makes direct contact with the organic semiconductor. Parameters of the gate dielectric, such as thickness, dielectric constant, and surface energy, have significant effects on the device performance of the OFET. Hence, research around gate dielectrics has been attracting great interest since the birth of OFETs.

Most OFETs for the aim of academic research are fabricated by utilizing thermal SiO_2 layers as their gate dielectrics due to the good insulating property of SiO_2 and the easy commercial availability of SiO_2/Si wafers. However, OFETs based on thick SiO_2 layers usually have high operating voltages, for example, 60 V was required for the operation of a transistor with a 300-nm-thick SiO_2 gate dielectric as mentioned in Ref. [58]. High operating voltages of OFETs

can be reduced by using Si substrates with a thinner SiO_2 layer. Alternatively, high-k inorganic oxides, such as sputtered amorphous barium zirconate titanate (BZT, k=17.3) [12], Si_3N_4 (k=6.2) [59], Ta_2O_5 (k=21–27) [60–62], Al_2O_3 (k=8) [26], etc., have also been used to decrease operating voltages. However, the manufacturing complexity of high-k inorganic compounds is a disadvantage of this approach.

Furthermore, polymeric dielectrics, which can be prepared by using low-cost large scalable solution processes, are important for the realization of mechanically flexible OFETs. The most serious problem of polymeric dielectrics is their low insulating property. It is difficult for common polymers to obtain a thin pinhole-free film without gate leakage currents [17,63]. Lately, some groups tried to tackle this problem by utilizing cross-linking polymer dielectrics to enhance the electrical robustness of polymeric gate dielectrics [64–68]. This may be a prospective direction for the development of soluble high-k polymeric insulators.

Besides the insulating property of gate dielectrics, more and more research works indicate that the surface quality of gate dielectrics has an impact on device performance as well. In 2002, Klauk *et al.* modified the surface of the SiO_2 gate dielectric with a self-assembled monolayer (SAM) of octadecyltrichlorosilane (OTS) [14]. The resulting pentacene-based OFETs achieved a field-effect mobility of 1 cm^2/Vs and a low threshold voltage of -1 V. Lei *et al.* did similar works in OFETs with polymeric semiconductors and also obtained enhancement on device performance [69].

A disadvantage of SAM modification is complicated processes for the monolayer. A simple alternative method is to insert a thin buffer layer instead of the SAM on the top of a gate dielectric. The thickness of this film is so small that it will not change bulk properties of the whole gate dielectric. For instance, Baeg *et al.* reported OFETs with improved device performance by using buffered nonpolar polymeric films, such as polystyrene (PS), poly(α-methylstyrene) (PαMS), and poly(methyl methacrylate) (PMMA) [70, 71].

2.1.1.3 Electrodes and Substrates

Compared to inorganic semiconductors, the conductivity of organic semiconductors is closer to insulators than to conductors due to the difficulty of doping [5]. For an OFET, charge carriers that form its conducting channel are injected from the source electrode under a proper bias on its gate. The injection of charge carriers is strongly dependent on the relative position between the Fermi level of

the source electrode and the molecular orbital of the organic semiconductor. If the Fermi level of the electrode is located close to the highest occupied molecular orbital (HOMO) (p-type) or to the lowest unoccupied molecular orbital (LUMO) (n-type) level of the organic semiconductor, that is, the contact energy barrier is low enough for the injection of charge carriers of one particular polarity, charge carriers can be injected when applying a voltage between the gate and the electrode, forming a conducting channel in the semiconductor layer. However, if the energy barrier height is large for both types of charge carriers, the organic semiconductor layer is nearly non-conductive due to the lack of mobile carriers. Therefore, the choice of electrode materials has to consider their matching performance with the semiconductor.

For devices based on pentacene, a typical electrode material is gold (Au) due to the small energy barrier between its work function and the HOMO level of pentacene. Other materials like silver (Ag) [72], copper (Cu) [73], molybdenum (Mo) [74], have also been utilized in later reports.

Furthermore, issues at the electrode/organic semiconductor interface also need to to be taken into account, especially for top-contact devices. For instance, during the high-temperature deposition process of electrodes, the diffusion of hot metal particles into the organic semiconductor layer may alter its molecular ordering and thus affect device performance. Some relevant effects will be discussed in Chapter 5. Deeper research can be also found in Refs. [75, 76].

The gate electrode, which is often attached intimately to the substrate or is the substrate itself, also plays an important role in OFET operation. The choice of gate materials is largely dependent on application requirements. For example, deeply doped Si substrates are primarily used in research works due to their easy availability with a natural gate dielectric of SiO_2, mechanical robustness, and superior conductivity. In contrast, indium tin oxide (ITO), which is a conductive metal oxide, has already been used in many areas of both research and industry, due to its two main advantages: easy fabrication in large areas and optical transparency. Substrates with deposited ITO thin films are thus more popular to be used as the gate electrode/substrate combination for the fabrication of flexible OFETs [77].

2.1.2 Device Geometric Structures

An OFET has three electrodes, namely gate, drain, and source. Depending on relative positions of electrodes and processing orders, there are four different structures of OFETs, as shown in Fig. 2.2.

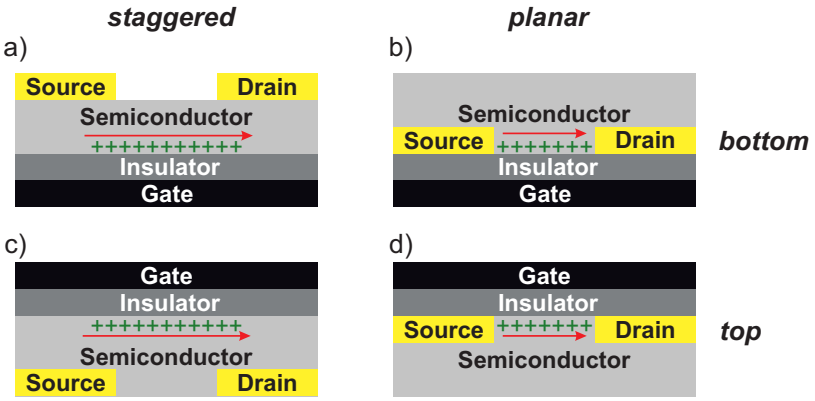


Figure 2.2. Illustrations of four structures of p-type OFETs. The carrier channel is plotted by green "+". (a) Bottom-gate staggered (b) Bottom-gate planar (c) Top-gate staggered (d) Top-gate planar.

According to the position of gate, OFETs can be categorized into bottom- and top-gate. The former has a gate electrode underneath the semiconductor layer, as shown in Fig. 2.2(a) and (b). Usually in these structures, the gate electrode is the substrate or pre-deposited on the substrate, e.g. deeply doped silicon wafers or ITO glasses. Convenient availability and processing simplicity are the most attractive advantages of bottom-gate structures. However, the natural connection of gate electrodes of all OFETs in one batch makes it difficult to build flexible circuits. In contrast, in top-gate structures the gate electrode is located on the top of the semiconductor layer (Fig. 2.2(c) and (d)). This structure is convenient for the fabrication of integrated circuits due to the simple preparation of gate lines via photolithography. In addition, top gate and gate dielectric layers can protect the sensitive semiconductor layer from influences of ambient conditions [78,79]. Nevertheless, the disadvantage of top-gate structures

is also very clear. The deposition of a gate dielectric layer on the top of the organic semiconductor may influence the functionality of the active layer.

Depending on the position of drain and source electrodes, OFETs can be also classified as staggered or planar. An OFET has a staggered structure, if its electrodes are separated from the gate dielectric (Fig. 2.2(a) and (c)). On the contrary, if its electrodes are attached directly to the gate dielectric, the transistor has a planar structure (Fig. 2.2(b) and (d)). According to the 2-D device simulation for OFETs reported by Shim *et al.* [80], staggered OFETs have better current injection than planar ones, because the effective area for injected currents at the electrodes/organic semiconductor contact in staggered structures is much larger than that in planar structures. This advantage is reflected by the reported high field-effect mobilities of the OFETs, which were mostly built with staggered structures [81–83]. However, the bottom-gate planar architecture (Fig. 2.2(b)) has its advantages, especially for the application of large-area fabrication, since the gate dielectric layer and metal electrodes can be prepared by photolithography with high resolution to increase the density of integrated OFETs [84, 85].

For the aim of basic theoretical research, it is preferred to utilize the bottom-gate staggered architecture (Fig. 2.2(a)), which benefits from simple manufacturing processes and stable high device performance. With this device geometry, more concentration can be put on understanding carrier transport and discussing the potential application of OFETs. Consequently, OFET devices in this thesis are fabricated with the bottom-gate staggered structure.

2.1.3 Basic OFET Operation

If we take a pentacene-based OFET (p-channel) with the bottom-gate staggered structure (Fig. 2.2(a)) as an example, its basic operation can be described as follows. When a negative voltage V_{GS} is applied between the gate and source electrodes, holes are induced at the source/pentacene interface. If these holes gain enough energy from the electric field built by V_{GS}, they can be injected into the pentacene layer by overcoming the relatively low energy barrier between Au work function and HOMO level of pentacene. As $|V_{GS}|$ increases, more and more holes accumulate at the lower part of the pentacene layer and form a conductive channel there. If another negative voltage V_{DS} between the drain and source electrodes is applied at the same time, the injected holes can be driven from source to drain electrode, which results in a current I_{DS}. The value of I_{DS} is

controlled by V_{GS}, which determines the amount of accumulated charge carriers, and V_{DS} when the absolute value of V_{DS} is small.

We can see that the OFET has a similar operation to metal-oxide-semiconductor field-effect transistors (MOSFETs), with the difference that there are no inverted doped wells in OFETs. Furthermore, the concept of p-type or n-type organic semiconductors is also different from the one of doping in conventional semiconductors. Whether an organic semiconductor is said to be p-type or n-type depends on the relative difficulty of hole injection and electron injection. If the injection of holes is easier and the conductive channel is formed by holes, this material is a p-type organic semiconductor. In contrast, if the injection of electrons is easier and the conductive channel is formed by electrons, the material is called an n-type organic semiconductor. There are also so-called ambipolar organic semiconductors, which can transfer both types of charge carriers [86].

2.1.4 Electrical Characteristics of OFETs

To investigate electrical properties of an OFET, two important current-voltage (IV) curves are often measured: output curve and transfer curve. Output curves exhibit the relationship between V_{DS} and I_{DS} for different V_{GS}. In Fig. 2.3, a set of output curves of a p-type OFET is demonstrated as an example. The

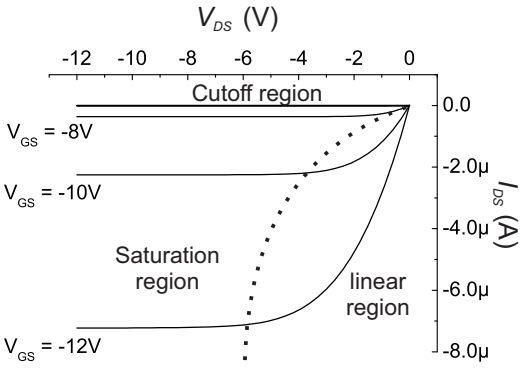


Figure 2.3. Measured output characteristics of a pentacene-based OFET with 30 μm channel length for different V_{GS}. For $V_{GS} > -8V$, the transistor is switched off.

output curves can be divided into three regions: cutoff region, linear region, and

saturation region. On the other hand, a transfer curve describes the relationship between V_{GS} and I_{DS} at a constant V_{DS}. In Fig. 2.4, the corresponding transfer curve for the p-type OFET in the saturation region is displayed by the blue curve in logarithmic y axis. We can see that the IV-curves of the OFET have similar forms to that of a MOSFET. Hence, it is preferred to use the current equations of MOSFETs to describe IV-characteristics of OFETs for the sake of simplicity [87, 88].

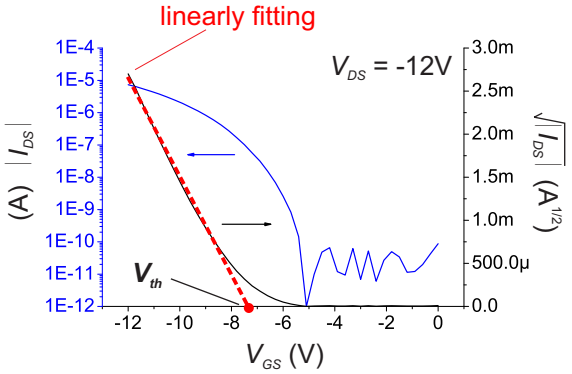


Figure 2.4. Measured transfer characteristics of a pentacene-based OFET with 30 μm channel length in the saturation region (V_{DS} = -12V). The blue curve demonstrates the output current I_{DS} in a logarithmic y axis (right). The black line indicates the square root of I_{DS}, which can be approximately fitted by a linear function (red curve). The intercept of the fitting curve on the x axis is defined as the threshold voltage V_{th} of the OFET in the saturation region. The slope of the fitting curve can be used to determine the field-effect mobility μ_e of the OFET.

Specifically, I_{DS} in a p-channel OFET can be determined by:

$$I_{DS} = \begin{cases} -\frac{W}{L}\mu_e C_i'[(V_{GS}-V_{th})V_{DS} - \frac{(V_{DS})^2}{2}] \text{for} \begin{pmatrix} V_{GS} \leq V_{th} \\ V_{DS} > V_{GS} - V_{th} \end{pmatrix} & (2.1) \\ -\frac{W}{2L}\mu_e C_i'(V_{GS}-V_{th})^2 \quad \text{for} \begin{pmatrix} V_{GS} \leq V_{th} \\ V_{DS} \leq V_{GS} - V_{th} \end{pmatrix} & (2.2) \end{cases}$$

where C_i' is the capacitance per unit area of the gate dielectric, W is the channel width, and L is the channel length. (IV-characteristics of n-channel OFETs

have the same formulas with opposite signs of voltages and currents.) Field-effect mobility μ_e and threshold voltage V_{th} are two important parameters that can be extracted from the transfer curve of the OFET.

Microscopically, carrier mobility μ characterizes how fast a charge carrier can move through a solid-state material under an electric field E and is defined as:

$$v = \mu E \tag{2.3}$$

where v is the velocity of the charge carrier. For a FET, the field-effect mobility μ_e indicates the speed of carrier transport inside the semiconductor layer, containing the influence of gate geometry and electric field effects [89]. The value of μ_e can be dependent on gate voltages and is always smaller than the real carrier mobility. According to the current equations, there are two ways to estimate the μ_e. In the linear region, where the small $|V_{DS}|$ makes $(V_{DS})^2/2 \ll |(V_{GS} - V_{th})V_{DS}|$, μ_e is estimated by measuring the slope of the linear transfer curve, as Eq. 2.1 can be approximated to:

$$I_{DS} \approx -\frac{W}{L}\mu_e C_i' V_{DS}(V_{GS} - V_{th}) \tag{2.4}$$

In the saturation region, where I_{DS} is independent of V_{DS}, μ_e is estimated by measuring the slope of the $\sqrt{|I_{DS}|}$-V_{GS} curve, as Eq. 2.2 can be reformed to:

$$\sqrt{|I_{DS}|} = \sqrt{\frac{W}{2L}\mu_e C_i'}(V_{GS} - V_{th}) \tag{2.5}$$

In practice, the calculated μ_e in different regions might show a deviation, which is located in an acceptable range. Hence, μ_e in the saturation region will be regarded as the default option in this thesis for the simplicity of discussion.

Threshold voltage V_{th} is actually a concept from Si-MOSFETs. It is defined as the gate bias, under which an inversion charge layer starts to be formed in the channel of a transistor [90]. Since OFETs do not operate in inversion mode but in accumulation mode, there exists no real threshold voltage. This concept is used here to describe the required minimal V_{GS} at which a conductive channel of accumulated charge carriers forms. The V_{th} can be extracted by measuring either the x-intercept of the linear transfer curve according to Eq. 2.4, or the x-intercept of the $\sqrt{|I_{DS}|}$-V_{GS} curve according to Eq. 2.5 (as shown in Fig. 2.4). Similar to μ_e, threshold voltage V_{th} in the saturation region will be mainly discussed within the frame of this dissertation.

With the help of the current equations, the output current I_{DS} of a p-channel OFET can be determined with respect to different voltage conditions. When $V_{GS} > V_{th}$, the output current is very low and can be neglected, as shown in Fig. 2.3. The transistor is considered to be off because no enough charge carriers are accumulated in the organic semiconductor layer. When $V_{GS} \leq V_{th}$, an output current I_{DS} can be observed. For small values of $|V_{DS}|$, I_{DS} is determined by Eq. 2.1. In this region, $|I_{DS}|$ increases almost linearly with $|V_{DS}|$. For large $|V_{DS}|$, especially when $|V_{DS}|$ is larger than $|V_{GS} - V_{th}|$, I_{DS} becomes independent of V_{DS} according to Eq. 2.2, as shown in Fig. 2.3. The reason is that the increasing horizontal electric field between the drain and source electrodes results in a low concentration of mobile charges near the drain. After the drain and the gate have the same potential, the channel will pinch off at this point and a further increasing of $|V_{DS}|$ will not increase $|I_{DS}|$ anymore [91]. This region is thus called the saturation region.

2.2 OFET-based Nonvolatile Memory Cells

Electronic memories can be divided into two main groups, depending on whether stored information will be lost or not when supply power is removed, namely volatile memories and nonvolatile memories. The commonest volatile memories are random access memories (RAMs), which have very fast write/erase/read dynamics. They are used as temporary storage units that exchange data with microprocessors at very high speeds. However, stored data in RAMs has to be regularly refreshed. On the other hand, nonvolatile memories have the capability to hold saved data when their power is switched off. This type of electronic memory device is therefore widely used for the long-lasting storage of mass data. Typical nonvolatile memory devices are read-only memories (ROMs), electrically erasable programmable read-only memories (EEPROMs), and flash memories.

Recently, new demands on using nonvolatile memories as date storage units embedded in stand-alone systems are emerging. In particular, organic electronic devices like RFIDs or medical sensors are implemented on flexible substrates and have relatively simple functions, it is preferable to integrate compatible memory units made of organic materials to improve their portability. Therefore, organic nonvolatile memories (ONVMs) are of great practical interest.

Within the framework of this dissertation, OFET-based ONVM cells will be discussed as application of OFETs. There are also other types of ONVM cells, e.g. resistive switching memories and capacitive memories, whose detailed reviews can be found in Ref. [92].

2.2.1 Basic Concepts of Organic Nonvolatile Memory Cells

In an OFET-based ONVM cell, the effect of charge storage usually occurs in its gate dielectric. By applying a large bias on the gate, charge carriers can be injected into the gate dielectric and get captured by trapping sites that are isolated from the semiconductor layer and the gate electrode. This trapping effect is quasi-permanently. The stored charge shifts the transfer curve of the OFET towards more positive or more negative, depending on the polarity of the charge carriers. A positive shift of the transfer curve is schematically shown in Fig. 2.5 as an example.

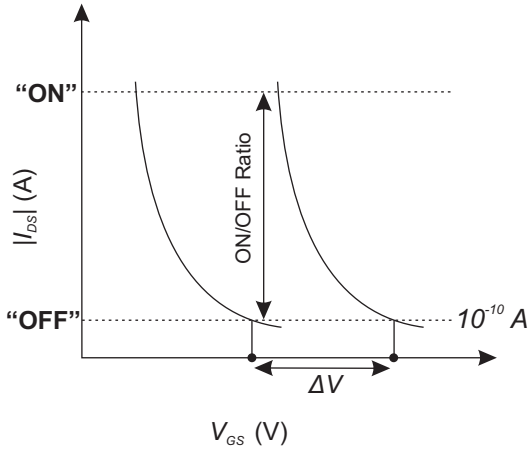


Figure 2.5. Schematic of the shift of transfer curve that denotes the memory window ΔV and the memory ratio. "ON" and "OFF" depict two current states before and after the gate bias, respectively.

The width of the shift in transfer curve is defined as the memory window ΔV, which is tightly related to the storage capability of a memory cell. ΔV is estimated by measuring the difference between the turn-on voltage after the programming process and the one after the erasing process. The turn-on voltage

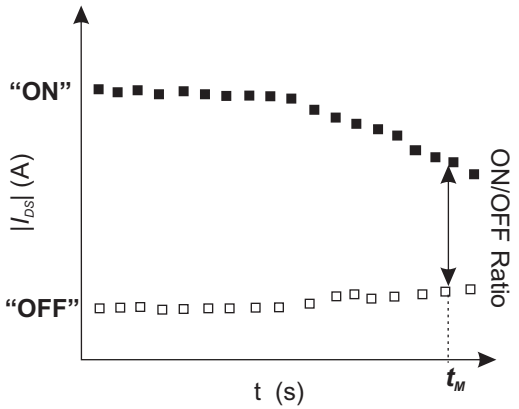


Figure 2.6. Schematic of the transient output currents that denotes the retention time t_{RE} and the memory ratio. "ON" and "OFF" depict two current states.

is the gate-source voltage V_{GS} at which the output current of the transistor exceeds 100 pA. I_{DS} at a fixed V_{GS} before and after applying the gate bias can be measured and regarded as the "ON" current and the "OFF" current, respectively. The memory ON/OFF ratio is thus given by the ratio between "ON" and "OFF" currents.

Ideally, the current state can be read non-destructively and remain until an opposite gate bias is set on. However, the memory ON/OFF ratio gradually declines over time because the stored charges can be released from the trapping sites due to the internal electric field. The ability of a memory cell to retain stored data is reflected by the retention time t_{RE}, which is defined as "the time interval between the instant that data is stored and the instant that the data can no longer be read correctly", according to IEEE standard definitions and characterization of floating gate semiconductor arrays [93]. However, the measurement of t_{RE}, whose definition is tightly related with digital circuits, is not practical for ONVM cells. Most research groups in the community prefer to assess the charge retention property of an ONVM cell by observing the memory ON/OFF ratio after a long measurement time t_M, as schematically exhibited in Fig. 2.6.

Additionally, the functionality of a nonvolatile memory can be damaged by program and erase operations due to permanent damages caused by high electric

fields. The endurance property describes the maximal tolerance of a memory device under repetitive cycles of program/erase operations.

2.2.2 Three types of OFET-based ONVMs

With respect to storage mechanism, there are three typical approaches for the realization of the gate dielectric of an OFET-based nonvolatile memory cell, namely gate dielectrics with embedded conductive nanoparticles (floating gate), ferroelectric gate dielectrics, and polymeric electrets, as displayed in Fig. 2.7. In following subsections, we will have a brief look at these three types of ONVMs.

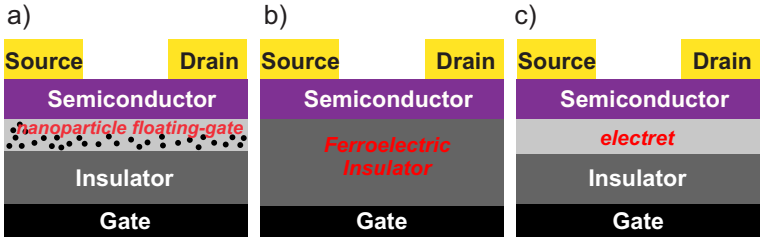


Figure 2.7. Schematic of ONVM devices based on (a) nanoparticle floating gates, (b) ferroelectric gate dielectrics, and (c) electrets.

2.2.2.1 Nanoparticle Floating Gates

Nanoparticle floating-gate ONVMs have a similar architecture to conventional inorganic nonvolatile memory devices, where a conductive floating electrode is completely surrounded by insulators. Injected charge carriers are stored in the floating gate and remain there even after the gate bias is removed. The difference in such organic memories is that the floating gate usually refers to discrete metallic nanoparticles or π-conjugated molecules, which are uniformly distributed in the gate dielectric. Each of the particles works individually as a charge-storage site. Hence, particle density in the floating gate determines the memory capability of the device, and its charge retention property relies on dielectric features of the insulating layer that separates floating particles from the active layer and the gate electrode.

Pioneer ONVMs with floating gates were realized by using Au nanoparticles due to their high chemical stability and possibility of solution processes [94].

Au nanoparticles can be prepared either by vacuum thermal evaporation processes [95–97] or by SAM solution processes [79, 98–101]. Compared to the thermal evaporation process, solution-based manufacturing processes are more suitable for large-scale fabrication and thus are more attractive for commercial applications. Other noble metals or metallic oxides (Ag, Pt, and Al/Al_2O_3 etc.) have also been utilized via similar methods to construct floating gates [96, 102–104].

It has to be noted that the density of metal nanoparticles is hard to increase due to the leakage effect caused by the high conductivity of these particles. Therefore, some recent research works are focusing on using trapping sites with relatively low conductivity. For instance, Xu *et al.* utilized organic semiconductor molecules C_{60} as nanoparticle floating gates, which could be manufactured synchronously with the tunneling layer. A large memory window of 8 V on average and switching endurance of more than 100 program/erase cycles were obtained [42]. Other attempts, such as quantum dots based floating gates [40] and nanofibrous floating gates [105], also showed good storage performance. However, the preparation of nanoparticles is still too complicated and energy consuming. For instance, the thermal evaporation of metal particles normally requires very high processing temperature, and the SAM technology requires long processing duration and specific experimental conditions.

2.2.2.2 Ferroelectric Gate Dielectrics

Another type of OFET-based ONVMs is the organic ferroelectric field-effect transistor (FeFET), whose gate dielectric shows a property of electric polarization [32]. The polarization is attributed to the alignment of intrinsic dipole moments in ferroelectric materials. The direction of the dipoles can be controlled by an external electric field and remains quasi-permanently after the electric field is removed. This aligned polarization forms a potential difference that induces either positive or negative counter charges in the semiconductor channel, resulting in an initial onset voltage, which can be reversed by applying an opposite electric field. The difference between the modified and reversed onset voltages thus creates different logic states for the output current of the transistor.

In 2004, the first all-organic FeFET device using pentacene as semiconductor was reported by Schroeder *et al.* [35], who deposited a ferroelectric-like polymer of poly(m-xylylene adipamide) (MXD6) as the gate dielectric. The memory ON/OFF ratio of this device was reported as between 30 and 200, and could be retained for around three hours. With almost the same memory ON/OFF

ratio and charge retention property, FeFETs using poly(vinylidene fluoride-trifluoroethylene) P(VDF-TrFE) as the gate dielectric were reported to have faster switching time [106]. That is one of the reasons why later research works on organic ferroelectric transistors mostly utilized polyvinylidene fluoride (PVDF) and its copolymer (P(VDF-TrFE)). In 2005, for example, Naber *et al.* reported using P(VDF-TrFE) (65:35) as the gate dielectric and a solution-processed polymer poly[2-methoxy-5-(2-ethyl-hexyloxy)-p-phenylene-vinylene] (MEH-PPV) as the active layer [18] . This device showed large hysteresis under programming voltages of 60 V or higher. The ON/OFF ratio of drain currents at zero gate voltage reached 10^4 and could be retained for one week. The programming time was as short as 0.3 ms.

This type of ONVMs also has several shortages, such as large leakage currents, high operating voltages, large surface roughness due to the semi-crystalline structure of P(VDF-TrFE), and a large residual depolarization field. Especially, the residual depolarization field, which is caused by insufficient charge carriers near the semiconductor/gate dielectric, noticeably worsens data retention.

2.2.2.3 Polymeric Electrets

ONVMs built with polymeric electrets are also called charge-trapping ONVM cells. They are realized by applying a so-called electret as the gate dielectric or a part of it. Injected charge carriers get captured in the electret or at its interface to the gate dielectric [107]. Compared to nanoparticles in floating-gate structures, electret layers are continual and amorphous [108]. They can be smoothly deposited by solution-based processes. Thus, the simple manufacturing of electrets is a clear advantage. Furthermore, the surface of electrets is usually friendly for the deposition of semiconductor films atop it. This is because most electrets are non-polar polymers with low surface energies, which are proven to be helpful for the ordering of deposited semiconductor molecules [71,109]. Lastly, since trap states are discrete energy levels in the gate dielectric, the probability of short circuits among stored charge carriers is thus very low, which contributes to a good charge retention property.

One of the first ONVM devices with electrets was reported by Baeg *et al.* in 2006 [70]. In this work, they reported a pentacene-based ONVM with a bilayer gate dielectric of poly(α-methylstyrene) (PαMS) and SiO_2. PαMS is a non-polar hydrophobic polymer, which has very low surface energy. The field-effect mobility of the transistor exceeded 0.5 cm^2/Vs. The device showed a large

memory window of about 90 V under a programming voltage of 200 V and the stored charge could be retained for more than 100 h. Their work also revealed critical issues that should be taken into account for the future commercialization of this memory type. Firstly, operating voltages for charge-trapping OFETs are usually very high. Secondly, programming efficiency is still low and should be further enhanced, including a larger memory window, faster programming time, and lower programming voltages. Last but not least, memory parameters, such as charge retention property and endurance behavior, are still far away from values of commercial flash memories or EEPROMs, which can keep the stored information for more than 10 years and be operated by more than 10^6 cycles of program/erase.

Within the framework of this dissertation, charge-trapping ONVM cells are extensively discussed as potential application of OFETs. In Chapter 5, OFETs with buffered polymer layers are explored as nonvolatile memories to investigate influences of different structural parameters and the operation mechanism of this memory type. Furthermore, possible strategies to optimize charge-trapping ONVM devices will be discussed in Chapter 6.

Chapter 3

Experimental Details for Device Fabrication and Characterization

3.1 Fabrication Techniques

This section gives a review of technologies utilized for the fabrication of OFETs. Compared to conventional inorganic semiconductor technologies, manufacturing processes of organic transistors are significantly simpler. There are three main types of techniques, namely substrate preparation, thin-film deposition, and patterning.

3.1.1 Substrate Preparation

Substrate preparation techniques include cleaning, drying, heating, etc. Since thicknesses of functional films in OFETs are usually in the range of tens of nanometers, the substrate for their fabrication should exclude any impurities larger than those films. Otherwise, undesirable particles might disturb or even disable the functionality of the device.

For the fabrication of OFETs in this dissertation, a standard cleaning process is performed for the preparation of every substrate. The cleaning procedure is carried out in a flow box with a ventilation system, and can be described as follows. First, raw substrates are cleaned sequentially by acetone and isopropanol in an ultrasonic bath for certain time. Acetone functions as a major cleaning agent, which is used to dissolve plastics, oil, fat, and other impurities. Another liquid – isopropanol – is applied as a supplementary cleaning agent to

remove residual acetone on substrates. Second, the cleaned substrates are rinsed by flowing distilled water to remove the organic cleaning agents. At last, the substrates are dried by N_2 blow and heated in a vacuum oven by increasing its temperature to more than 100 °C. This cleaning process is suitable for chemically and thermally robust materials, such as Si/SiO_2 substrates or ITO glass substrates. For sensitive substrates, such as paper or polyesters, the utilized cleaning agents and heating temperature have to be chosen carefully.

Furthermore, UV/ozone treatment on the cleaned substrates is a special preparation technique that follows the cleaning process. Such a treatment is performed by illuminating the substrates with ultraviolet radiation of different wavelengths (185 and 254 nm) in a black box. The light of 185-nm wavelength converts the atmospheric oxygen (O_2) into ozone (O_3), whereas the 254-nm light dissociates O_3 back to O_2 and singlet atomic oxygen, which has strong oxidation power and reacts with the substrates. Through this reaction, residual organic impurities on their surfaces can be removed as volatile products like O_2, CO_2, and H_2O, while the inorganic substrates are oxidized and covered by some new molecules or chemical groups, such as C-O, OH, C-O=C, etc., which may change chemical properties of their surfaces.

3.1.2 Deposition of Thin Films

Available deposition techniques for OFETs can be classified into two categories: solution-based deposition and thermal evaporation deposition. They are applied to generate functional thin films that build an OFET. Two specific techniques used in this dissertation are reviewed as follows.

Spin coating

Spin coating is a widely used solution-based coating method for soluble polymers and other materials. Its advantages include the ability for large-scale application and processing simplicity. In this thesis, the spin-coater WS-650 LITE from *Laurell Technologies Corporation* is used for all spin-coating processes. The work mechanism of a spin-coating process is illustrated in Fig. 3.1.

The target material for the coating process is previously dissolved in a solvent, which can easily volatilize at room temperature. Then, a certain amount of the prepared solution is applied on the center of a substrate, which is fixed on a turntable rotating at a steady speed, normally 2000 - 3000 rpm. The

solution falling on the substrate is spread out instantly and uniformly by the centrifugal force. As the rotation continues, excess fluid spins off the edge of the substrate, and the solvent starts to evaporate. This way, a homogeneous film of the target material is formed on the surface of the substrate. The thickness of the coated film mostly depends on the viscosity and concentration of the solution, the angular speed of spinning, and the duration of spinning [110]. After the rotation is stopped, some residual solvent still exists in the wet layer. Therefore, it is usually necessary to heat the substrate in a vacuum oven to get rid of the residues.

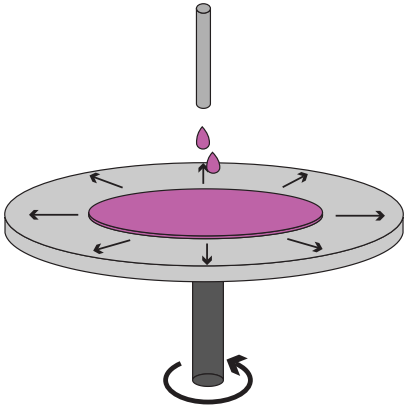


Figure 3.1. Schematic of the spin-coating process

Thermal evaporation

Thermal evaporation belongs to physical vapor deposition (PVD) techniques, which only change physical states of deposited materials and induce no chemical reaction. Thermal evaporation processes in this thesis are carried out with the Mini-Coater 1709MinCo010 from *tectra GmbH*. The basic mechanism of this technique is interpreted schematically in Fig. 3.2.

A thermal evaporation process occurs in a high vacuum chamber. The target material for the coating process is prepared in a metallic or quartz boat that has an extremely high melting point. By heating the boat via electrical currents, the solid material melts and evaporates. Material vapors with high temperature

isotropically diffuse into the upper space of the chamber. A substrate is fixed by a substrate holder relatively wide from the boat, and remains cool with the help of a closed-cycle cooling system inside the holder. When the hot vapors reach the cold substrate, they are solidified and thus form a thin film on the surface of the substrate. The thickness of this deposited layer is controlled during the deposition process by a quartz crystal sensor with the help of a SQM-160 Rate/Thickness monitor from *INFICON Inc.* The displayed thickness value is estimated by using a tooling factor that is determined by the relative position between substrate holder and material boat in the evaporation equipment.

Thermal evaporation is used widely in research works of OFETs because it can deposit a smooth thin film of molecular organic semiconductors with crystalline or polycrystalline structures, which contribute to high carrier mobilities. The quality of the deposited thin film depends on various deposition parameters, including the purity of the deposited material, deposition temperature, air pressure in the chamber, substrate temperature, and deposition rate.

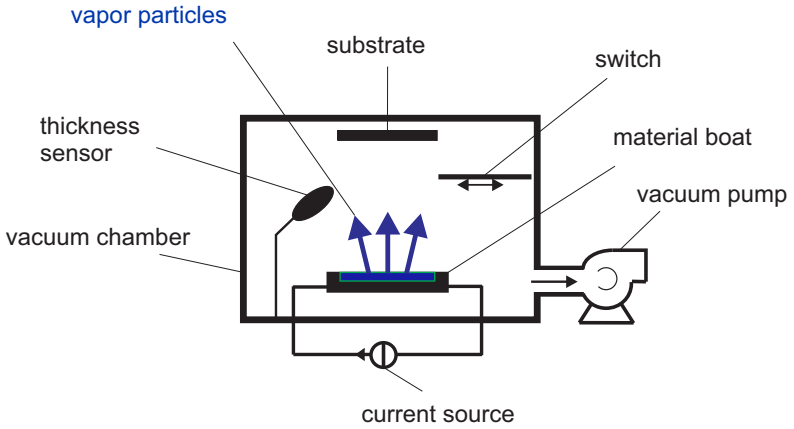


Figure 3.2. Schematic of the evaporation process

3.1.3 Patterning

Patterning refers to techniques that form the geometrical structure of functional films. Usual patterning techniques in semiconductor industry are photolithography and etching, which can achieve fine resolutions in the nanometer range. However, they are also the most expensive techniques due to high-priced lithography machines and plasma etching systems.

Considering the relatively large channel length of OFETs (30 μm) in this thesis, a simple patterning technique using a shadow mask is applied. The shadow mask is in physical contact with a substrate. For a thermal evaporation process, a compact package containing the mask and the substrate is brought together into the deposition equipment. Part of the substrate surface is passivated by the mask, whereas the other part is exposed to material vapors. Thereby, a film of the target material is deposited with a structure formed by the shadow mask during the deposition process. The resolution of the shadow mask can reach tens of micrometers, which can well satisfy requirements of OFETs in this dissertation. Moreover, another reason for this physical patterning technique is the difficulty in choosing proper photoresists for photolithography because many organic materials are also dissolved in solvents of photoresists.

3.2 Measurement Techniques

Measurements in three aspects are undertaken in this dissertation to characterize OFET and ONVM devices, namely the morphology of thin-film surfaces, the electrical performance of transistors, and memory behavior. This section introduces mechanisms of measurement techniques as well as applied measurement equipments and platforms.

3.2.1 Morphological Properties of Thin Films

Surface energy and contact angle

Surface energy refers to the excess energy present at the surface of a solid and often reflects the wettability of a solid surface [111]. Many research works, such as [112], [27], and [109], reported that electrical properties of OFETs are strongly affected by the surface energy of their gate dielectrics due to its influence on the deposition of the organic semiconductor layer atop it. However, surface energy is

difficult to measure directly. The estimation of surface energy is usually realized by measuring contact angles of different liquids on a solid surface.

As shown in Fig. 3.3, the contact angle θ is defined as the angle at the intersection of the contour of a liquid drop with the plane of a solid surface. The contact angle originates from a force equilibrium of three tensions and has

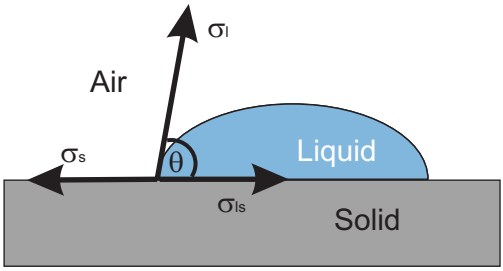


Figure 3.3. Schematic of the contact angle θ and surface energy. σ_s and σ_l represent the surface energy of the solid and the liquid, respectively. σ_{ls} denotes the interfacial tension.

the following relation with surface energies, according to the Young's equation:

$$\sigma_s = \sigma_{ls} + \sigma_l cos\theta \tag{3.1}$$

where σ_s, σ_l and σ_{ls} are the surface energy of solid, the surface energy of liquid, and the interfacial tension between solid and liquid, respectively. By measuring θ of at least two different liquids, whose surface energies are previously known, the surface energy of the solid can be determined.

In this work, a universal and high-quality Drop Shape Analyzer DSA 100 from *Kruess GmbH* is utilized to estimate surface energies of substrates in different conditions by measuring contact angles of two liquids, namely water and glycol ethylene, which are commonly used for SiO_2 substrates and polymers.

Surface roughness

Surface roughness is another important factor for thin films that needs to be taken into account. Especially for devices like OFETs, which consist of multiple thin films, a homogeneous and smooth surface of the layer underneath is impor-

tant for the deposition of upper layers. In general, microscopy is used to observe the morphology of solids. There are three primary types of microscopy, namely optical microscopy, electron microscopy, and scanning probe microscopy (SPM).

Atomic force microscopy (AFM) is a type of SPM with sub-nanometer accuracy and can be used to measure the surface roughness of a sample. The AFM XE-100 from *Park Systems Corporation* is applied for morphological measurements of SiO_2 substrates and polymers in this dissertation. In the AFM, there is a small cantilever, which has a sharp tip at its end. When the tip moves into the proximity of a sample surface, possible forces, such as the mechanical contact force, van der Waals forces, electrostatic forces, magnetic forces, etc., are imposed on the tip, leading to deflections of the cantilever. Since forces that work on the cantilever depend on the distance between cantilever and sample surface, areas with different heights or depths cause varied deflections of the cantilever. The changed deflections are detected by an optical system making use of the reflection of a laser beam on the cantilever. The deviation of the reflected laser beam enables a profiling of the sample surface. Hence, a topographic image of a certain area of the sample can be obtained by scanning the surface and recording the laser deviations. The average surface roughness of a thin film is then estimated by analyzing topographic images measured on different areas of the sample. More details about the operation principle of AFM can be found in other publications, such as [113] or [114].

Thin-film Thickness

Differentiated by different coating processes, there are two types of thin films within the framework of this dissertation, namely thermally deposited films and spin-coated films. On the one hand, the thickness of the thermally deposited film has to be measured before the first deposition attempt of the equipment or after changing the position of the substrate holder, in order to calibrate the thickness monitor. On the other hand, thicknesses of spin-coated films, including buffered polymers and electrets, also need to be determined to control parameters of spin-coating processes.

In this thesis, thicknesses of both types of thin films are all measured by the stylus profilometer Dektak 150 from *Veeco Instruments Inc.* The operation of the stylus profilometer is based on the scanning of a diamond stylus in contact with the sample under investigation. If the surface is covered partly by a film,

the vertical height at the edge of the film can be measured as its thickness. The measurement resolution of Dektak 150 can reach as small as few nanometers.

3.2.2 Electrical Measurements on OFETs

As discussed in Section 2.1.4, field-effect mobility and threshold voltage are the most important parameters that reflect the electrical performance of an OFET. Both parameters can be extracted from IV-characteristics of the OFET by using current equation 2.5. In this thesis, measurements of output and transfer curves are performed by a self-built system based on the semiconductor analyzer *Agilent* 4155C/4156C. The test platform is displayed in Fig. 3.4.

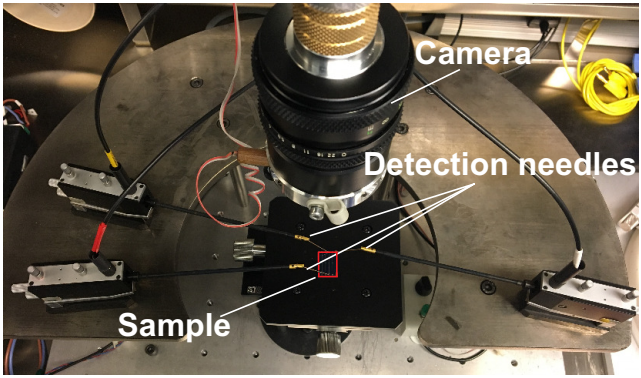


Figure 3.4. A photo of the measurement platform for the OFET.

Three detection needles at the end of micropositioner probeheads, which are connected to the semiconductor analyzer, make contact with the drain, source, and gate electrode of the device under test, respectively. The 4155C/4156C has four high-resolution source/monitor units (SMUs), each of which combines a source channel and a monitor channel together. Measurements of IV-curves are realized by performing the sweep measurement function of the 4155C/4156C. That is, source channels of SMUs perform different staircase sweep voltages (V_G, V_D, and V_S) to drive the transistor, while their monitor channels measure the output currents (I_G, I_D, and I_S) for each sweep step.

Specifically, to measure the transfer curve of a transistor, V_{DS} is constant and V_{GS} is swept once from the start value to the end value in small steps, as

shown in Fig. 3.5(a). To measure output curves of the transistor, V_{GS} is slowly stepwise increased, while V_{DS} cyclically varies for each step of V_{GS}, as shown in Fig. 3.5(b).

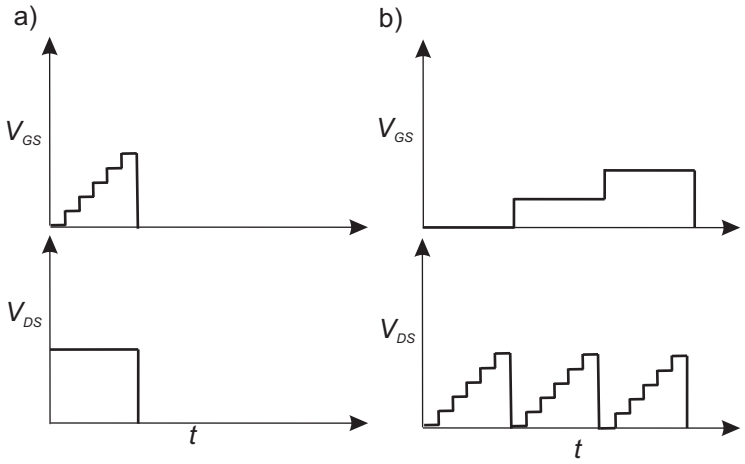


Figure 3.5. Typical transient schemes of sweep voltages from *Agilent* 4155C/4156C for measurements of (a) the transfer curve and (b) the output curve.

The operation of measurements is controlled by a self-programmed software supported by *Matlab* via computer connection, and measured results can be displayed simultaneously and saved as data files through the program.

3.2.3 Measurements of Memory Properties

To evaluate a nonvolatile memory device, memory window, charge retention property, and endurance behavior are the most important parameters. Detailed definitions of them are given in Sec. 2.2.1. Based on the testing platform for transistors, a specific platform for measurements of memory properties is built by adding the *Agilent* 41501A/B SMU/Pulse Generator Expander.

Memory window

The measurement procedure of memory window ΔV for a pentacene-based ONVM is demonstrated in Fig. 3.6.

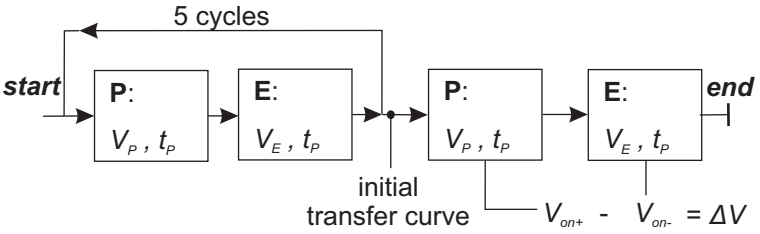


Figure 3.6. Measurement procedure for the memory window ΔV. "P" means the program step and "E" means the erase step. V_{on+} and V_{on-} are turn-on voltages of a memory cell in the programmed state and in the erased state, respectively. The definition of V_{on} is given in the text.

First, the device is initialized by five program/erase (P/E) cycles. Programming voltage V_P and erasing voltage V_E are generated by the 41501A/B and forced on the gate electrode of the ONVM cell. Since the injection difficulty of electrons and holes are different in the pentacene-based ONVM cell, the V_E can discharge or neutralize all the stored electrons caused by the V_P and inject extra holes into the trapping sites, so that the returned transfer curve is located more negative than its position before the programming process. In the next programming process, electrons injected by the V_P has to neutralize these stored holes, and thus less electrons are stored. This way, the transfer curve cannot reach the position that it reached after the first programming process. Similarly, the position of the returned transfer curve after the next erasing process can be shifted again. After certain times of P/E cycles, transfer curves in the erased state and in the programmed state gradually approximate to balanced positions, where the net charge caused by V_P (discharged holes and injected electrons) is equal to that caused by V_E (discharged electrons and injected holes). In this way, the memory has a stable memory window and supplies stable output current in different states under this set of V_P and V_E.

Second, a program signal with a positive voltage of V_P and a duration of t_P is sent onto the gate electrode. The transfer curve moves to the programmed state, consequently. Then, this transfer curve is measured to determine the turn-on voltage V_{on+} in the programmed state. As mentioned in Sec. 2.2.1, the turn-on voltage V_{on} is defined as the gate-source voltage V_{GS} at which the output current I_D reaches 100 pA.

Third, an erase signal with the same duration of t_P but a negative voltage of V_E is set onto the gate. The transfer curve thus moves back to its initial position.

V_{on-} denotes here the turn-on voltage after the erasing process. Finally, the memory window ΔV is given by the difference between V_{on+} and V_{on-}.

Charge retention property

The charge retention property of an ONVM cell can be indicated by measuring its output currents in the programmed state and in the erased state over a long period of time, separately. Time diagrams of input signals V_G and V_D for each measurement are demonstrated in Fig. 3.7(a) and (b), respectively. The source electrode of the memory cell is grounded for both measurements.

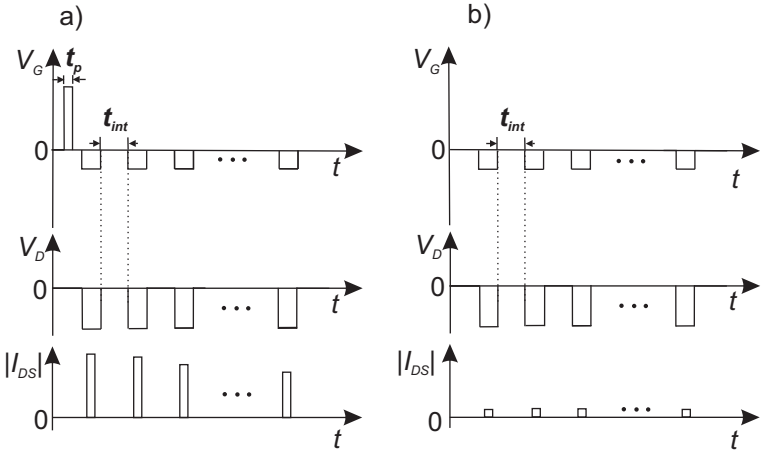


Figure 3.7. Input signals for the measurement of retention behavior in (a) programmed mode and (b) erased mode, where t_P and t_{int} represent the duration of gate pulse and the interval between two read steps, respectively.

For the measurement of the output current in the programmed state, the ONVM device is programmed by applying a gate bias V_P for t_P after the initialization process. Following, read voltages at the gate $V_{G,read}$ and drain $V_{D,read}$ are applied to the device, whose output current I_{DS} is measured by the semiconductor analyzer. Afterwards, the read process is repeated at a time interval of t_{int}, as shown in Fig. 3.7(a). In the idle time between two read steps, all electrodes are floating in order to minimize the influence of biased voltages on the stored charge. Similarly, the measurement of I_{DS} in the erased state can be realized by excluding the programming step after the initialization of the device,

as shown in Fig. 3.7(b). The charge retention property of the tested device is reflected by the change of the current ratio between programmed state and erased state in dependence of measurement time.

Endurance behavior

The measurement of endurance behavior of an ONVM cell is undertaken on the same platform for the measurement of charge retention property. The time diagram of input signal on each electrode is illustrated in Fig. 3.8. The source electrode of the memory cell is also grounded.

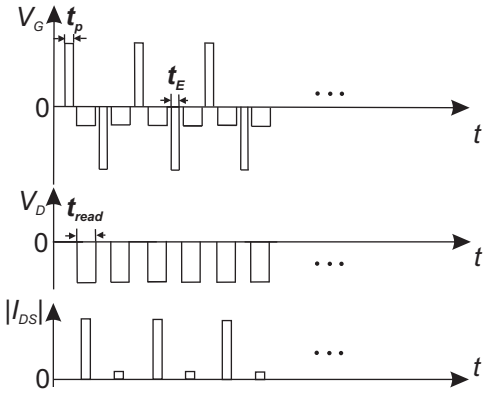


Figure 3.8. Input signals for the measurement of endurance behavior, where t_P, t_E, and t_{read} represent the duration of programming, erasing, and read process, respectively.

The measurement starts with an input of V_P for a duration of t_P on the gate, turning the memory cell into the programmed state. Shortly after the voltage stress, the semiconductor analyzer measures the output current I_{DS} within a read time of t_{read}. After the read process terminates, an erasing signal of V_E with a duration of t_E is sent onto the gate, turning the memory cell into the erased state. Following, the output current is read with the same set of voltages. The measurement continues by repeating the "program-read-erase-read" cycle. The endurance behavior of a nonvolatile memory can be described by the cycle number together with the current ratio between programmed state and erased state after operating the device for such an amount of P/E cycles.

Chapter 4

Surface Modification for Gate Dielectrics of OFETs

Research efforts to improve device performance of OFETs are concentrated mostly in the following aspects: choosing proper semiconductor materials, optimizing manufacturing processes, or modifying the gate dielectrics of OFETs. Among them, the modification of gate dielectrics, especially the modification of the gate dielectric surface, is an effective strategy to adjust the electrical properties of OFETs. In this Chapter, two simple manufacturing methods of surface modification are utilized and their influences on OFET performance are investigated, including field-effect mobility and threshold voltage.

In Sec. 4.1, OFETs are fabricated on a deeply n-doped Si substrate with a 300 nm film of thermally grown SiO_2, without any surface modification. Electrical properties of these OFETs are characterized as reference data for following discussions. In Sec. 4.2, comparative OFETs are fabricated on SiO_2 gate dielectrics buffered by different polymeric thin films. The inserted polymers change surface energies of the gate dielectrics, and influence field-effect mobilities of the OFETs. Afterwards, the effect of another type of surface modification – UV-ozone treatment – is investigated in Sec. 4.3. This treatment shows influences on both field-effect mobilities and threshold voltages. At last, mechanisms of surface modifications are discussed by comparing the electrical properties of modified OFETs with the results of non-modified OFETs.

Parts of the results in this chapter were published in conference proceedings of *18th International Conference on Organic Electronics 2016* in Singapore [115].

4.1 OFETs Fabricated on a pristine SiO_2 Substrate

The geometric structure of OFETs fabricated on a pristine SiO_2 substrate is illustrated in Fig. 4.1(a). The transistor consists of an active layer of pentacene, two Au electrodes, and a conductive substrate (Si n++) with a pre-deposited insulating layer of SiO_2. The heavily n-doped Si substrate with a 300-nm-thick dry thermal SiO_2 layer was purchased from *Silicon Materials GmbH*. Pentacene was purchased from *Merck KGaA* with a sublimed grade of more than 99.9 %. The channel length L is 30 μm and the channel width W is 1 mm, which are realized with the help of a shadow mask from *Ossila Ltd.*

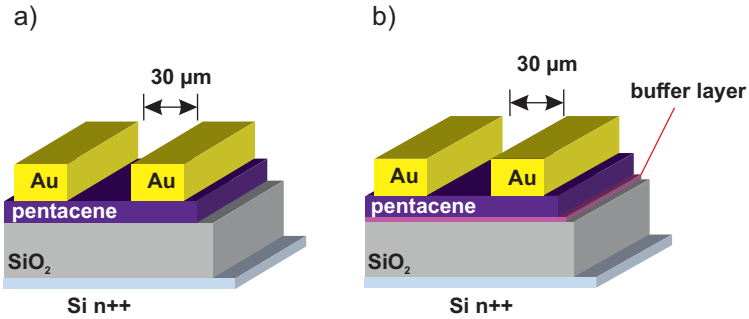


Figure 4.1. Schematic structures of OFETs fabricated on (a) a pristine SiO_2 substrate and (b) a polymer buffered substrate, respectively.

Experimental

OFETs were fabricated via the following procedure. First, the SiO_2 substrate was cleaned sequentially by acetone and isopropanol in an ultrasonic bath for 10 minutes each. Then, the substrate was rinsed by distilled water and dried by getting heated in a vacuum oven at 120 °C for at least 30 minutes. Second, the substrate was settled in a metallic package with structured open windows, through which only selected areas of the substrate surface would be covered by a pentacene layer during the following deposition process. The whole package was transferred into a thermal evaporator installed in a sealed glove-box with a nitrogen atmosphere. Pentacene was then deposited at a rate of 0.1 Å/s in the

evaporator under high vacuum conditions (pressure $P < 1 \times 10^{-6}$ mbar). The deposition rate and the deposited thickness of the pentacene layer were instantly measured by a quartz sensor. The target thickness of the pentacene layer for this experiment was 30 nm. Third, the substrate would be taken out from the evaporator after the deposition of pentacene, and transferred into another evaporator with a different, finely structured shadow mask. Afterwards, source and drain electrodes were formed by the deposition of Au in similar processing conditions. The thickness of Au was set to 50 nm. In this manner, five transistors were fabricated on the substrate, as shown in Fig. 4.2.

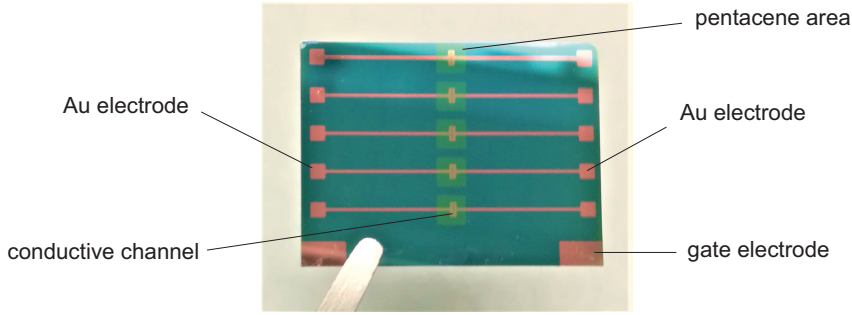


Figure 4.2. A photo of a substrate with five fabricated OFETs.

Characterization

For characterization, the substrate with five fabricated OFETs is placed on a test table, and electrode pads of a transistor are in contact with micropositioner probeheads, which are connected to the semiconductor analyzer *Agilent* 4155C/4156C. The measurement is undertaken according to the measurement protocol described in Sec. 3.2.2. Output and transfer curves of the transistor are characterized by using different sets of drain-source voltage V_{DS} and gate-source voltage V_{GS}, separately. Measurements are repeated for each functional transistor on the substrate by changing the contacted electrode pads. Measurement results are discussed as follows.

Fig. 4.3 demonstrates a set of output curves of a measured OFET as a typical example. It can be seen that the curves can be divided into three specific regions, namely cutoff region, linear region, and saturation region. For $V_{GS} \geq$ -20 V, nearly no current is observed in the whole range of V_{DS}, which means the transistor is turned off. For $V_{GS} <$ -20 V, the absolute value of the drain-source current $|I_{DS}|$ increases with the absolute value of the drain-source voltage $|V_{DS}|$, and the transistor finally reaches the saturation region, where $|I_{DS}|$ hardly changes with further increasing $|V_{DS}|$. In the saturation region, I_{DS} almost solely depends on V_{GS}. This OFET has a typical p-channel behavior, in which output currents can be observed only under negative V_{DS} and V_{GS}.

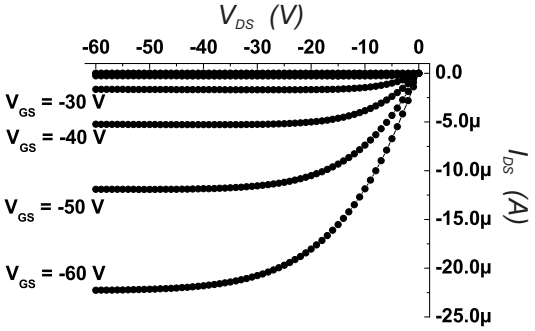


Figure 4.3. Output curves of an OFET fabricated on a pristine SiO_2 substrate.

Output curves mainly demonstrate the relationship between I_{DS} and V_{DS}, whereas transfer curves put more emphasis on the relationship between I_{DS} and V_{GS}. In Fig. 4.4(a) and (b), corresponding transfer curves of the transistor with V_{DS} = -0.5 V and V_{DS} = -60 V are demonstrated, respectively. In both figures, it can be seen that the tested pentacene-based OFET is initially turned off when no voltage or a positive voltage is applied on the gate. Only when the applied gate voltage becomes more negative than a critical voltage and a negative V_{DS} is given at the same time, a current starts to flow between the drain and source electrodes. For V_{DS} = -0.5 V, as shown in Fig. 4.4(a), I_{DS} almost has a linear form related to V_{GS}, i.e., the transistor is operated in the linear region. On the other hand, for V_{GS} = -60 V, $I_{DS} = f(V_{GS})$ approximates to a parabolic function, as shown in Fig. 4.4(b), indicating the saturation region of the OFET. In this experiment, Eq. 2.5 was applied to estimate field-effect mobilities μ_e and

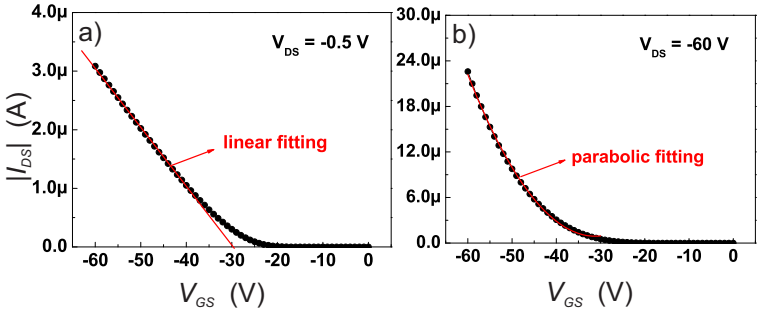


Figure 4.4. Transfer curves of a measured OFET fabricated on a pristine SiO_2 substrate in (a) the linear region (V_{DS} = -0.5 V) and (b) the saturation region (V_{DS} = -60 V). The red lines refer to different fitting functions.

threshold voltages V_{th} of OFETs in the saturation region. The mean value of the extracted μ_e is around 0.1 cm^2/Vs, and the average V_{th} is about -31 V.

Based on the fabrication of OFETs on the pristine SiO_2 substrate, two types of surface modifications will be applied to pristine SiO_2 substrates in the next two sections. In each section, experimental details of the corresponding surface modification are firstly given, and its influence on the device performance of OFETs is discussed subsequently.

4.2 Polymeric Buffer Layers

Polymeric buffer layers are widely utilized to modify substrate surfaces in OFET construction due to their high effectiveness and easy processability. Solution-based manufacturing processes for polymers are compatible with the fabrication of OFETs.

Experimental

In this experiment, different polymers, including polystyrene (PS), poly(α-methyl styrene) (PαMS), and polyvinyl alcohol (PVA), are applied as buffer layers. These materials were purchased from *Merck KGaA*. Polymer solids were dissolved in suitable solvents in advance, with concentrations of 0.5 wt% PS in toluene, 0.5 wt% PαMS in toluene, and 0.5 wt% PVA in distilled water. The

fabrication of OFETs with buffered gate dielectrics had a similar procedure to that described in Sec. 4.1. The only difference was that polymeric thin films were previously deposited on the top of pristine SiO_2 substrates via spin-coating processes, which were carried out in a flow box with ambient air. Parameters for each spin-coating process were kept the same, e.g. spinning duration at 60 s and rotation speed at 3000 rpm. Afterwards, the coated substrates were annealed in a heated vacuum oven for at least one hour. Parts of the modified substrates were used for surface measurement, and the remaining ones for OFET fabrication. After fabrication, field-effect mobilities μ_e and threshold voltages V_{th} of OFETs with different gate dielectrics were characterized by using the same test procedure as noted in Sec. 4.1.

Surface energy

Surface energies of the substrates after surface modification were estimated by measuring contact angles of two liquids that were dropped on their surfaces, as mentioned in Sec. 3.2.1. The measured water contact angles θ are displayed in Table. 4.1. Since contact angles of the other liquid – glycol ethylene – on

Table 4.1. Morphological and electrical characteristics of OFETs with different buffer polymers

Samples	Water contact angle θ (deg.)	Surface energy σ_s (mN/m)	Field-effect mobility μ_e ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	Threshold voltage V_{th} (V)
pristine SiO_2	73.5	36.2	0.1	-30.9
PαMS	93.1	25.1	0.7	-30.2
PS	90.8	28.4	0.6	-29.1
PVA	61.8	40.1	0.2	-28.9

these surfaces have the same tendency as water, only the water contact angles are mentioned in the discussion for simplicity. It can be seen that the substrates covered by PαMS or PS have an average θ of more than 90°, which is much larger than the θ on pristine SiO_2 substrates. In contrast, the substrate modified with a PVA film has a much smaller θ of around 62°. By applying Eq. 3.1, surface energies σ_s of the substrates with different buffer layers were calculated. The

results are summarized in Table. 4.1, and the relationship between σ_s and θ is illustrated as the black curve in Fig. 4.5.

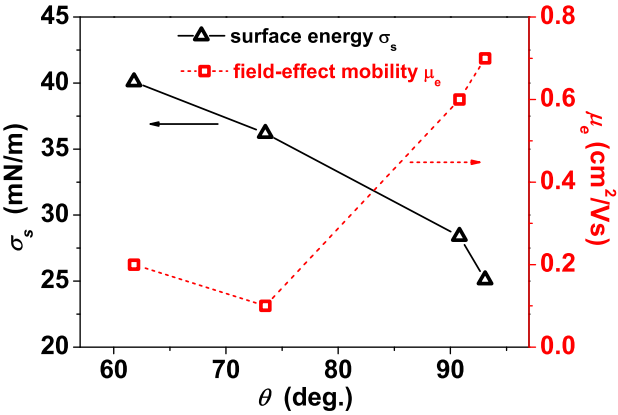


Figure 4.5. Measured surface energies σ_s (black triangles) and field-effect mobilities μ_e (red boxes) in Table. 4.1 related to the water contact angle θ. The triangle or box symbols are the average measured data of OFETs in one batch.

We can see that the surface energy of a solid σ_s decreases with the increasing contact angle θ. Since a small σ_s also indicates a low polarity of the material, polymers like PS and PαMS are therefore categorized into the group of non-polar materials, and PVA is oppositely a more polar polymer.

Electrical properties

Now, we are looking at electrical properties of the modified transistors. The extracted μ_e and V_{th} of OFETs with different gate dielectrics are presented in the last two columns of Table. 4.1. μ_e shows an approximately positive correlation with θ except the case of OFETs on the pristine SiO_2 substrate. As shown in Fig. 4.5, the value of μ_e reaches as high as 0.7 cm^2/Vs in devices with a large θ of about 93°, and declines to 0.2 cm^2/Vs when θ is reduced down to 62°. One exception is that the μ_e of transistors fabricated on the pristine SiO_2 substrate shows a lower value than any other devices with buffer layers. Besides, we see a negative correlation between σ_s and μ_e for transistors with buffer layers, i.e., the μ_e is reduced with increasing σ_s. On the other hand, threshold voltages V_{th} of all tested transistors are located in the small range of -31 to -29 V, where no

big changes are observed with respect to θ or σ_s.

By summarizing these results, it can be concluded that inserting a polymeric buffer layer on the gate dielectric can generally enhance the μ_e of an OFET in comparison with the one fabricated on the pristine SiO_2 substrate, and non-polar polymers that have low surface energies show better effects on the field-effect mobility. Moreover, this modification method has no noticeable impact on V_{th}.

4.3 UV-Ozone Treatment

Different approaches have been proposed to modify the V_{th} of OFETs over time, such as inserting self-assembled monolayer (SAM) [14, 25], O_2 plasma treatment [116], and UV-ozone treatment [16, 29, 30]. Among them, UV-ozone treatment is attractive due to no requirement of extra materials, simple manufacturing processes, and low processing temperature. In Ref. [117], Huang *et al.* reported their works by using UV-ozone treatment on PS gate dielectrics of the OFETs, which were fabricated on ITO glasses. In that work, the absolute value of V_{th} was gradually reduced by extending the treatment duration. Inspired by this work, UV-ozone treatment is adopted in OFETs with the PS-buffered SiO_2 gate dielectrics to investigate its influence on V_{th} and μ_e of the OFETs.

Experimental

The procedure for this experiment is based on the fabrication of OFETs with buffered gate dielectrics, as schematically shown in Fig. 4.6. Substrates were firstly covered by a thin film of PS and annealed in a heated vacuum oven for at least one hour. Then, the substrates were transferred into a UV-ozone ProCleaner^{TM} purchased from *Bioforce Nanosciences* to receive a UV-ozone treatment. In order to investigate the influence of the duration of treatment on device performance, the treatment time on each substrate was set differently, varying from 0 to 180 s. Following, the fabrication of OFETs was completed by depositing a pentacene layer and Au electrodes onto the prepared substrates, sequentially.

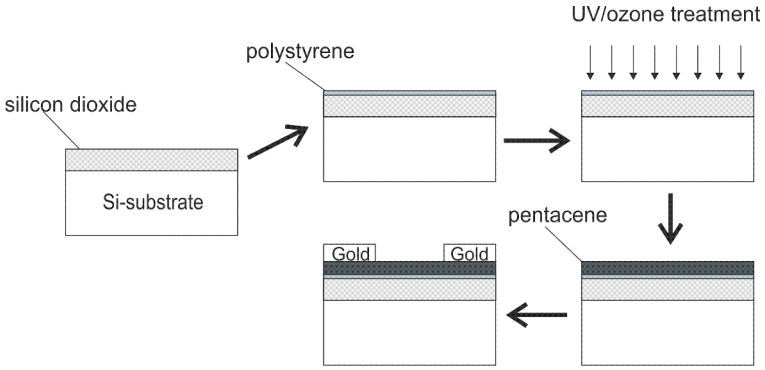


Figure 4.6. Schematic of fabrication of OFETs, adding the UV-ozone treatment before the deposition of pentacene.

Results

In Fig. 4.7, transfer curves of several OFETs with UV-ozone treatments are illustrated and compared to the transfer curve of a non-modified transistor fabricated on the pristine SiO_2 substrate.

It can be seen that the reference transistor has a more negative threshold voltage V_{th} (about -30 V) in comparison to the modified transistors. The transfer curve shifts towards positive values of V_{GS} with increasing duration of the treatment, showing a reduction of $|V_{th}|$. In addition, we can see that slopes of the transfer curves are also changing, implying that the UV-ozone treatment has changed the field-effect mobility μ_e of the OFETs as well.

V_{th} and μ_e of all OFETs under investigation were extracted from their transfer curves. The results are displayed in Fig. 4.8, in which V_{th} and μ_e are related to the UV-ozone treatment duration. The field-effect mobility of the reference transistor μ_{e0} is also plotted in the same figure. We can see that the average value of $|V_{th}|$ is reduced from about 29 V to nearly 10 V with increasing duration of UV-ozone treatment from 0 to 180 s. Particularly, a rapid change of V_{th} is observed within the first thirty seconds. When the treatment time further extends, the reduction of $|V_{th}|$ continues at a decreasing rate. As for the change of μ_e, we can see that the initial value of μ_e in PS-buffered OFETs without UV-ozone treatment is around 0.6 cm^2/Vs, which decreases to 0.2 cm^2/Vs after 30 s of UV-ozone treatment. However, with longer treatments, the value of μ_e

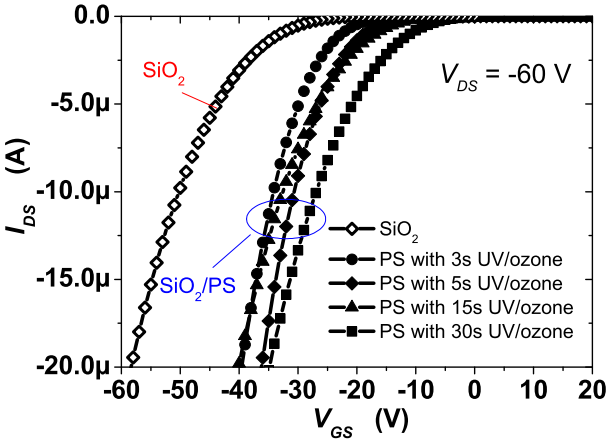


Figure 4.7. Transfer curves of OFETs fabricated on a pristine SiO_2 substrate and on a PS-buffered gate dielectric with UV-ozone treatments.

remains at approx. 0.2 cm^2/Vs, which is still higher than the one of the reference transistor.

The results indicate that UV-ozone treatment on OFETs with a PS-buffered gate dielectric of SiO_2 can not only reduce their $|V_{th}|$, but also decrease their μ_e. Nevertheless, the downward tendency of μ_e is stopped after 30 s of UV-ozone treatment and μ_e of the devices with UV-ozone treated PS-buffered gate dielectrics are still larger than the ones of the non-modified transistors on the pristine SiO_2 substrate.

4.4 Discussion on Mechanisms of Surface Modification

Influence on field-effect mobility μ_e

From the experimental results, it is confirmed that the surface modification of gate dielectrics does indeed influence the μ_e of OFETs. The mechanism of this phenomenon has been discussed in publications [109, 112, 118]. It is suggested that low surface energies of gate dielectrics facilitate the three-dimensional (3-D) growth of a pentacene layer, in which the deposited pentacene molecules tend to be gathered as small 3-D grains. This way, tight connections between neighboring grains and reduced discontinuous spaces in the pentacene layer lead to a better arrangement of the pentacene molecules. Consequently, the improved crystalline

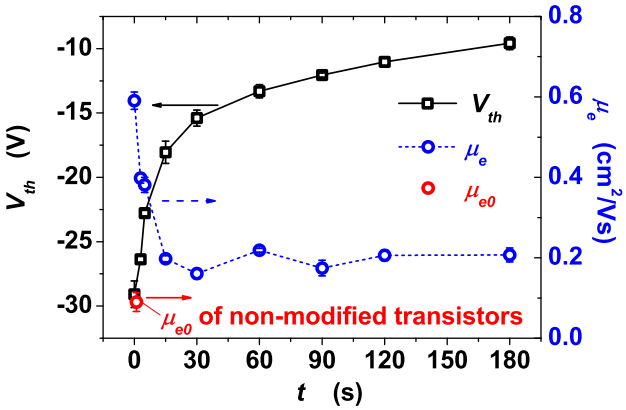


Figure 4.8. Threshold voltage V_{th} and field-effect mobility μ_e of OFETs with a gate dielectric of PS buffered SiO_2 related to the duration of UV-ozone treatment. The reference point indicates the average μ_e of OFETs fabricated on the pristine SiO_2 substrate. The connected points are mean values of measured results from the transistors in the same batch and the bars indicate the variations in different transistors.

structure of pentacene with less defects and charge traps promotes the transport of charge carriers and thus enhances μ_e. Inserting non-polar buffered polymers, such as PS and PαMS, on gate dielectrics reduce the surface energy of the gate dielectric, and thus resulted in higher μ_e. On the other hand, modifying gate dielectrics with the polar polymer PVA or treating gate dielectrics with UV-zone illumination, which increases the wettability and thus the polarity of the treated surface, has negative influences on the μ_e of OFETs due to increased surface energy.

However, this conclusion is only confirmed under the condition that the comparative OFETs have the same type of gate dielectric surface. Even though the surface energy of a PVA-buffered gate dielectric or a UV-ozone treated PS-buffered gate dielectric is higher than that of a pristine SiO_2 substrate, field-effect mobilities of those modified OFETs were still observed to be larger than the one of non-modified OFETs. In fact, the deposition of pentacene also depends on the chemical structure of the gate dielectric surface [19, 63]. The surface of an organic polymer naturally has more similarity to the structure of pentacene than the surface of SiO_2, because both polymers and pentacene layers have molecular structures, whereas SiO_2 has an atomic structure [27]. The affinity between polymers and organic semiconductors facilitates a better arrangement of pen-

tacene molecules [69, 119–121]. Moreover, UV-ozone treatment might change the alignment of energy levels between polymeric surfaces and pentacene near their interface as reported in [30], which also affects the field-effect mobility of an OFET. Therefore, surface energy is not the only factor that influences the μ_e of OFETs with different types of gate dielectrics. Only when all other factors are kept constant, lowering the surface energy of a gate dielectric can surely improve the μ_e of the OFET.

Influence on threshold voltage V_{th}

According to [86] and [122], UV-ozone treatment stimulates chemical reactions with the buffered PS layer and introduces oxygen groups, such as C-O, C=O and O-C=O, onto the surface of the gate dielectric. These functional groups exhibit high electron-trapping effect, and act as fixed negative charges after capturing electrons [123]. When a gate voltage is applied on the OFET, more holes will be induced at the semiconductor/gate dielectric interface to balance the fixed negative charges [116, 124], Consequently, the V_{th} is positively shifted. Since the density of the introduced oxygen groups is determined by the duration of the UV-ozone treatment, the shift of V_{th} thus depends on the treatment time.

The electron traps induced by UV-ozone treatment have aroused high interest. They behave like quasi nonvolatile storage sites, which are very inspiring for possible application of OFETs as nonvolatile memory cells. First of all, the positive shift of the V_{th} of a p-type transistor is of practical interest for the realization of a low-voltage memory device. Second, a single-transistor structured memory cell has good compatibility with transistor-based logic circuits. Last but not least, manufacturing processes of this device are very simple without much difference from fabricating an OFET. However, the V_{th} shift of the above-mentioned device is uncontrollable due to the easy neutralization of stored charges with the semiconductor layer. If an OFET is going to be adopted as a writable memory cell, its threshold voltage is supposed to be controlled by an extra gate bias after the device fabrication. Therefore, the main task for the realization of ONVM devices based on this type of OFETs is to isolate the stored charge from the semiconductor layer.

Chapter 5

Structural Parameters Affecting the Memory Behavior of ONVMs

This chapter introduces basics of charge-trapping ONVM cells as well as their fabrication steps. Then, impacts of Au thickness and electret thickness on memory behavior will be investigated in Sec. 5.2 and 5.3, separately. The results show that by increasing the Au thickness of an OFET-based ONVM cell, its memory window is enlarged due to better injection of electrons at the Au/pentacene interface. As for the influence of the electret thickness, one observes a tradeoff between programming efficiency and charge retention property. Furthermore, the mechanism of charge storage in charge-trapping ONVM cells is discussed by comparing memory behavior of devices with different structural parameters.

Parts of the results in this chapter have been published in Ref. [58].

5.1 Application of OFETs as ONVMs

5.1.1 Charge Trapping in Gate Dielectrics

Fundamentally, OFET-based charge-trapping ONVMs are realized by separating the semiconductor layer from the gate dielectric with a so-called electret layer, as shown in Fig. 5.1.

In the electret or at the dielectric/electret interface, there exist charge-trapping sites, which originate from specific chemical groups (e.g. C-O, C=O, O-C=O, hydroxyl). When a gate bias voltage is applied, charge carriers are

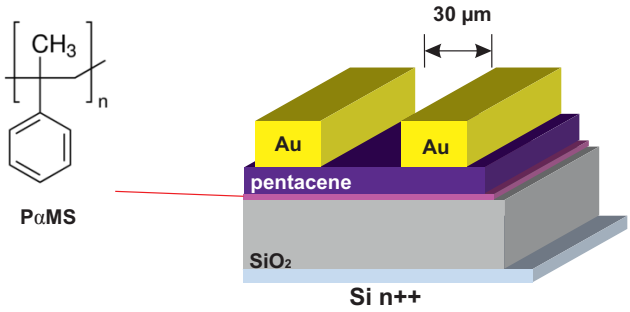


Figure 5.1. Schematic of the structure of an ONVM device with PαMS as its electret layer.

injected into the semiconductor layer, tunnel through the electret film and eventually get captured by the trapping sites [36, 107]. The storage of the charge carriers can be retained quasi-permanently due to the isolation of these trapping sites. Two major events occur during this process, namely charge injection and charge trapping. Sufficient injection of one type of charge carrier is required to obtain an effective memory window in the OFET device. In pentacene-based OFETs, which have negative threshold voltages V_{th}, the injection of electrons is more preferable, because it causes a positive shift of V_{th} which avoids high operating voltages. However, the injection of electrons is actually impeded in this type of OFETs by the significant energy barrier between the work function of Au and the lowest unoccupied molecular orbital (LUMO) level of pentacene [125]. Therefore, the efficiency of electron injection in pentacene-based ONVMs needs to be enhanced. The charge-trapping process occurs after the injection of charge carriers. The thickness of the electret layer directly influences the tunneling process of the charge carriers. Furthermore, since trapping sites are located in the electret or at the electret/gate dielectric interface, the choice of electret material and surface properties of the electret also determine the density of traps and trapping efficiency of a memory cell. In general, the influence of the mentioned events is reflected in various parameters, such as memory windows, charge retention property, and endurance behavior.

Many research works have focused on the electret film, such as utilizing different electret materials [39, 126–128], designing novel structures of electrets

[39,43,129], or managing surface treatments on electrets [130]. Recently, the work of Ling *et al.* [38] provided an insight into the dependence of the memory window on the electret thickness, whereas its influence on the charge retention property of a memory cell has been not elucidated yet. Furthermore, very few studies have investigated the impact of charge injection, which also plays an important role in memory behavior. Further studies on both aspects of charge injection and charge trapping are beneficial to the understanding of storage mechanisms.

In this work, charge-trapping ONVM devices are fabricated by utilizing poly(α-methylstyrene) (PαMS) as electret. PαMS is a non-polar polymer, which can modify the surface of a gate dielectric to achieve high μ_e (see results in Sec. 4.2). Compared to similar non-polar styrenic polymers, such as polystyrene (PS), poly(4-methyl styrene) (P4MS) or poly(2-vinyl naphthalene) (PVN), ONVM devices with PαMS as the electret have the best programming efficiency, according to a report from Baeg *et al.* [71]. Therefore, discussions in the following sections are based on the same electret material of PαMS.

5.1.2 Fabrication of ONVM Devices

ONVM cells were fabricated on a deeply n-doped silicon wafer (Si n++) with 300 nm SiO_2 on top. Materials, such as pentacene (sublimed grad > 99.9 %, HOMO $\sim$ 5 eV, LUMO $\sim$ 3 eV) and PαMS (Mn $\sim$ 427,000), were purchased from *Merck KGaA*. The purchased PαMS is semi-transparent powder, which was dissolved into toluene solvent to prepare solutions in advance. The wafer was cut into substrates with a size of 20 $\times$ 15 mm. The fabrication procedure is described as follows.

At first, the substrates were cleaned by acetone and isopropanol sequentially in an ultrasonic bath for 10 min each, rinsed by distilled water, dried by N_2 blow, and then heated in a vacuum oven for 30 min. Following, all the substrates were covered by a thin film of PαMS via spin-coating processes at a rotation speed of 3000 rpm for 1 min. Solutions with different concentrations of PαMS from 0.5 wt% to 2 wt% were applied on different substrates to obtain films of thicknesses from 12 to 45 nm. The coated substrates were baked in a vacuum oven at 120 °C for 1 h, subsequently. Next, a 30-nm-thick film of pentacene was deposited on top of each PαMS-coated substrate. This process occurred at a deposition rate r_p of around 0.5 Å/s in a high vacuum chamber (pressure P $<10^{-6}$ mbar), which is embedded in a nitrogen filled glove-box from *MBraun*. Finally, Au electrodes were deposited and structured through a shadow mask at

a low deposition rate r_{Au} of 0.1 Å/s in another chamber under the same level of high vacuum. The fabricated memory devices have a top-contact bottom-gate structure, and all transistors have the same channel length and channel width, namely $L = 30$ μm and $W = 1$ mm.

5.1.3 Characterization of ONVM Devices

The characterization of ONVM Devices is divided into two parts: the measurement of electrical properties and the measurement of memory behavior. In the case of electrical properties, output curves and transfer curves of the pentacene-based OFETs are measured by using the method that is described in Sec. 3.2.2. Parameters, such as V_{th} and μ_e, can be extracted from the transfer curves.

For the measurement of memory behavior, two factors - memory window ΔV and charge retention property - are investigated. As defined in Sec. 2.2.1, ΔV describes the shift of the transfer curves between two logic states. This is one of the most important factors that indicate the storage ability of a nonvolatile memory cell. The measurement protocol for the estimation of ΔV in Sec. 3.2.3 is applied. Two measurement parameters that should be considered carefully are programming time t_P and programming voltage V_P. ONVM devices requiring lower V_P or/and shorter t_P to obtain a certain level of ΔV indicate higher programming efficiency. On the other hand, the charge retention property of a nonvolatile memory cell indicates its ability to retain stored data. The numerical parameter used to depict the charge retention property of conventional flash memories is retention time t_{RE}. However, since the measurement of t_{RE}, whose definition (given in Sec. 2.2.1) is tightly related with digital circuits, is not practical for ONVMs, most research groups in the community prefer to assess the charge retention property of an ONVM cell via observing the memory ON/OFF ratio for a relatively long period of time. The memory ON/OFF ratio describes the ratio of output currents between two logic states. In this chapter, output currents in the "ON" state and in the "OFF" state of tested devices are measured for 10^3 s, separately. The charge retention property of devices can be thus demonstrated by their transient current curves.

In Sec. 5.2, electrical properties and memory windows are compared and discussed among devices with the same electret thickness d_e and varied electrode thickness d_{Au}. In Sec. 5.3, devices with the same d_{Au} and different d_e are analyzed with an emphasis on programming efficiency and charge retention property.

5.2 Influence of Au Electrode Thickness

To examine the relation between Au thickness d_{Au} and memory window ΔV, different ONVM cells with $d_{Au} = 25$ nm, $d_{Au} = 35$ nm, and $d_{Au} = 45$ nm, are fabricated and investigated. Other parameters of fabrication remain the same for all devices ($d_e = 12$ nm, $r_p = 0.5$ Å/s, $r_{Au} = 0.1$ Å/s).

In Fig. 5.2(a)-(c), we can see transfer curves of three transistors with d_{Au} of 25 nm, 35 nm, and 45 nm, respectively. In each diagram, the black curve displays the transfer curve of a device in its initial state, whereas the red line is the transfer curves after the programming process and blue line the transfer curve after the erasing process. Programming time t_P is set to 1 second and programming voltage V_P is kept at 100 V. It can be seen that the shift of the transfer curve ΔV increases with rising d_{Au}. In total, OFETs of three batches have been characterized in this experiment. Each batch comprises five transistors with the same d_{Au}. The average values of ΔV and field-effect mobility μ_e are summarized in Fig. 5.3.

We can see that μ_e of transistors (red squares) with different d_{Au} remain in a small range around 0.7 cm^2/Vs, whereas ΔV (black points) continually increases with d_{Au}. Specifically, at $d_{Au} = 25$ nm, ΔV almost vanishes with a mean value of 2.2 V, while the average ΔV of devices with $d_{Au} = 35$ nm and $d_{Au} = 45$ nm are 13.7 V and 16.6 V, respectively. The results show that the thickness of Au electrodes plays a noticeable role in the ΔV of a memory device. Generally, Au electrodes influence the memory behavior of top-contact OFET-based ONVM cells in two aspects. They will be explained separately as follows.

Interface dipole

Since the SiO_2 layer in the fabricated ONVM cells is too thick to tunnel through, stored electrons, which cause the transfer curve shift of the ONVM cells, are mainly injected from Au electrodes. In other words, the injection of electrons occurs at the Au/pentacene contact. In the case of an ideal contact, as shown in Fig. 5.4(a), the work function of Au (Φ_{Au}) is close to the highest occupied molecular orbital (HOMO) of pentacene (an energy barrier ϕ_h of approx. 0.1 eV). This feature contributes to easy injection of holes under negative gate voltages, which matches with the p-channel semiconductor behavior of pentacene. In contrast, the injection of electrons is quite poor due to the high energy barrier between Φ_{Au} and the lowest unoccupied orbital (LUMO) of pentacene ($\phi_e \approx$

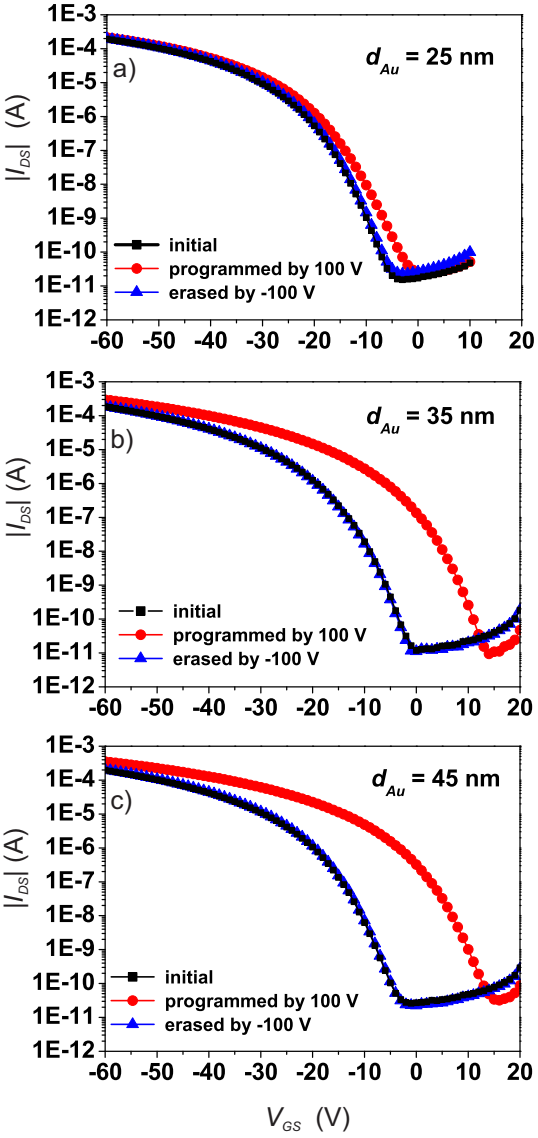


Figure 5.2. Programming/erasing characteristics of transistors with d_{Au} = (a) 25 nm, (b) 35 nm, and (c) 45 nm. It can be seen that the width between initial transfer curve and programmed transfer curve is increasing from (a) to (c). The erased transfer curves nearly overlap with the initial curves due to the initialization process of the measurement.

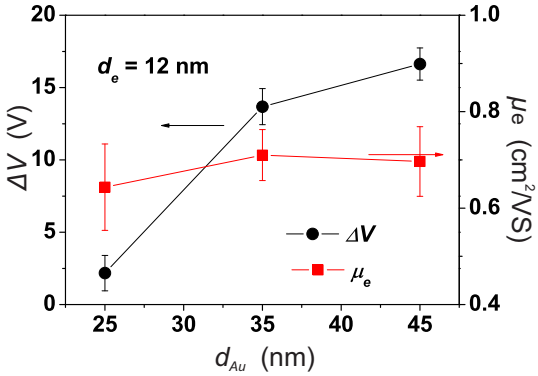
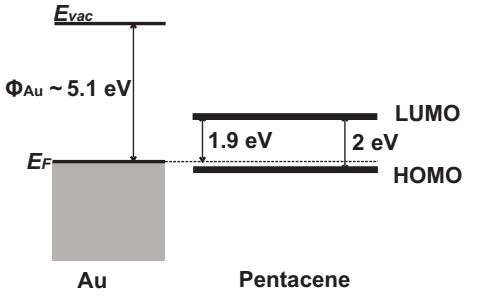


Figure 5.3. Relationship between d_{Au} and ΔV as well as μ_e. The solid points represent mean values of measured data and the error bars indicate standard deviations of measured data.

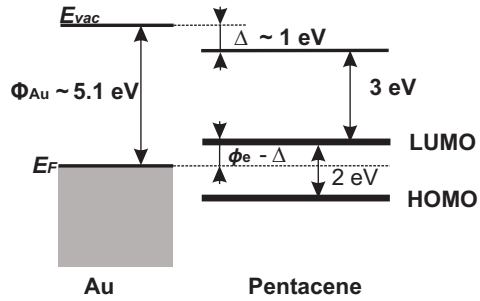
1.9 eV) [131]. The poor electron injection unfortunately hinders the memory performance of an ONVM cell, because few electrons can reach the trapping sites in the electret or at its interface to the gate dielectric of the ONVM cell. However, in the non-ideal case, the contact between Au electrodes and pentacene in a top-contact OFET can be altered as mentioned in Ref. [73, 132]. Making contact between metal and molecular surface forms interface dipoles Δ, which equally yield a shift of the vacuum level of the organic semiconductor with respect to the metal [131, 132]. This Δ can be up to 1 eV in the case of depositing Au onto the pentacene surface, as shown in Fig. 5.4 (b). The formation of interface dipoles lowers ϕ_e and thus enhances the injection of electrons, which enlarges the memory window of the memory cell.

Diffusion and gap states

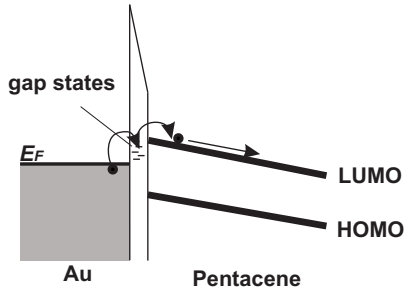
Metal diffusion is another process that influences the injection of electrons. When the high-temperature Au deposition process is performed at low deposition rates, Au particles can diffuse into the pentacene film [73, 134, 135]. The hot Au particles can alter the polycrystalline structure of the pentacene film in the upper region, and induce gap states at the interface [136]. These gap states facilitate the promotion of electrons into transport levels in pentacene, as shown in Fig. 5.4(c).



a) ideal case (V_{GS} = 0 V)



b) real case (V_{GS} = 0 V)



c) real case (V_{GS} > 0 V)

Figure 5.4. Energy schemes of an Au/pentacene contact at (a) ideal case, (b) real case $V_{GS} = 0$ (adapted from [131]). (c) For $V_{GS} > 0$, the induced gap-states assist the injection of electrons. The reference data of Au work function Φ_{Au} is cited from Ref. [133]. The data of pentacene HOMO and LUMO levels are given by the material supplier *Merck KGaA*.

Since increasing d_{Au} introduces more particles that arrive at the Au/pentacene interface [76], the Au diffusion is thereby enhanced. With the enhanced Au diffusion, more gap states are introduced at the interface. The injection of electrons is therefore improved by increasing d_{Au}. However, it must be noted that an oversized Au electrode might introduce undesirable cross leakage currents in the channel with a short length [75], which should be carefully considered in practice.

In summary, d_{Au} influences the memory behavior of an ONVM cell mainly through its impact on the injection of electrons. By increasing the thickness of deposited Au electrodes, ΔV of ONVM cells can be effectively increased due to the enhancement of electron injection at the Au/pentacene contact.

5.3 Influence of Electret Thickness

Apart from the injection of electrons, which is mainly influenced by d_{Au}, charge trapping is another important event that determines the memory performance of ONVM cells. As mentioned in Sec. 5.1.1, injected electrons tunnel through the electret layer and stop either at the electret/SiO_2 interface or in the electret. The thickness of the electret layer d_e affects both transport and storage of the electrons.

In this section, ONVM cells with different d_e (approx. 12 nm, 20 nm, 28 nm, 36 nm and 45 nm) are prepared by changing the concentration of PαMS in the toluene solution, while all other fabrication parameters remain the same (d_{Au} = 45 nm, r_p = 0.5 Å/s, r_{Au} = 0.1 Å/s). Memory behavior of these ONVM cells is investigated in two aspects: memory window and charge retention property.

5.3.1 Characterization of Memory Window ΔV

Measurement results

As explained in Sec. 5.1.3, programming voltage V_P and programming time t_P are two parameters that should be taken into account for the measurement of ΔV. Firstly, the ΔV of the tested memory cells were measured by applying varied V_P in the range of 60 to 200 V with a fixed t_P = 1 s.

The results displayed in Fig. 5.5 show the relation between ΔV and V_P for each d_e. It can be seen that all curves have a similar tendency: starting with an inactive region at small values of V_P, increasing rapidly when V_P exceeds a

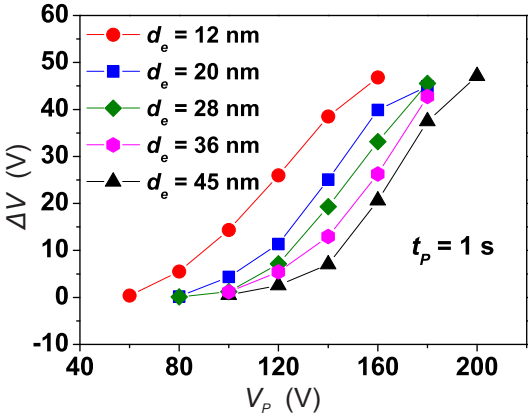


Figure 5.5. ΔV of devices with different thicknesses of electret d_e related to varied V_P within a fixed $t_P = 1$ s.

critical value, and growing slowly at large values of V_P. Generally speaking, ΔV increases with V_P, which is self-evident. However, $\Delta V = f(V_P)$ curves do not overlap each other but shift towards higher V_P with increasing d_e, which implies that the ΔV of a memory device dose not solely depend on V_P.

If ΔV of different devices are compared under the same V_P, for instance, at $V_P = 100$ V, we can see that ΔV decreases from 14.4 V to almost zero when increasing d_e from 12 nm to 45 nm, as illustrated in Fig. 5.6. The result reveals that increasing d_e hinders electrons tunneling through the electret layer, leading to fewer stored electrons that contribute to ΔV.

Secondly, ΔV of two devices with representative d_e (thin $d_e = 12$ nm and thick $d_e = 28$ nm) were investigated by applying varied t_P under a fixed V_P of 100 V, 120 V, 140 V, and 160 V, separately. The results are demonstrated in Fig. 5.7. For each V_P, ΔV of both devices show similarly an increase at the beginning and gradually reach a saturated value. Even though the device with a thin electret reaches the saturation of ΔV faster, final values of ΔV in both devices are approximately the same. The results seem to tell us that d_e has no effect on ΔV if the memory device is programmed by a long enough t_P. To interpret results from the above two measurements, the charge storage dynamics of this type of ONVM devices should be carefully discussed.

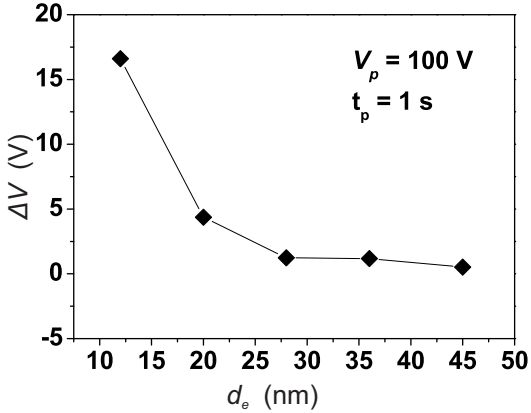


Figure 5.6. ΔV of devices with different d_e at $V_P = 100$ V and $t_P = 1$ s. It can be seen that ΔV decreases with increasing d_e.

Charge storage dynamics

It is well known that ΔV is caused by the stored charge Q, which has the following relation with the total gate capacitance C_t:

$$\Delta V = \frac{Q}{C_t} \tag{5.1}$$

where C_t can be regarded as two capacitors in series. Since the dielectric oxide has a much larger thickness (300 nm) relative to d_e in this work, C_t is mainly determined by the thick SiO_2 film and can be treated as constant in all ONVM cells for simplicity. Hence, ΔV becomes approx. proportional to Q, i.e., to the integral of the current during the programming process. The current density J is caused by the internal electric field E_e across the electret. Since the conductivity of PαMS is very low, J is negligible for low E_e. When E_e exceeds a critical value of E_{e0}, the probability of charge carriers penetrating the PαMS film near the interface increases. The mechanism of carrier transport in the insulated electret depends on its thickness d_e [137].

For an ultrathin electret film ($d_e < 10$ nm), as illustrated in Fig. 5.8, electrons can reach the PαMS/SiO_2 interface via a tunneling process, in which J is merely determined by E_e and the barrier height $\Delta\phi$ at the pentacene/PαMS contact [90]. This tunneling process, which is also described as the fast-charging process of an ONVM cell, takes place instantly within a time scale of 10^{-6} to 10^{-4} s [138].

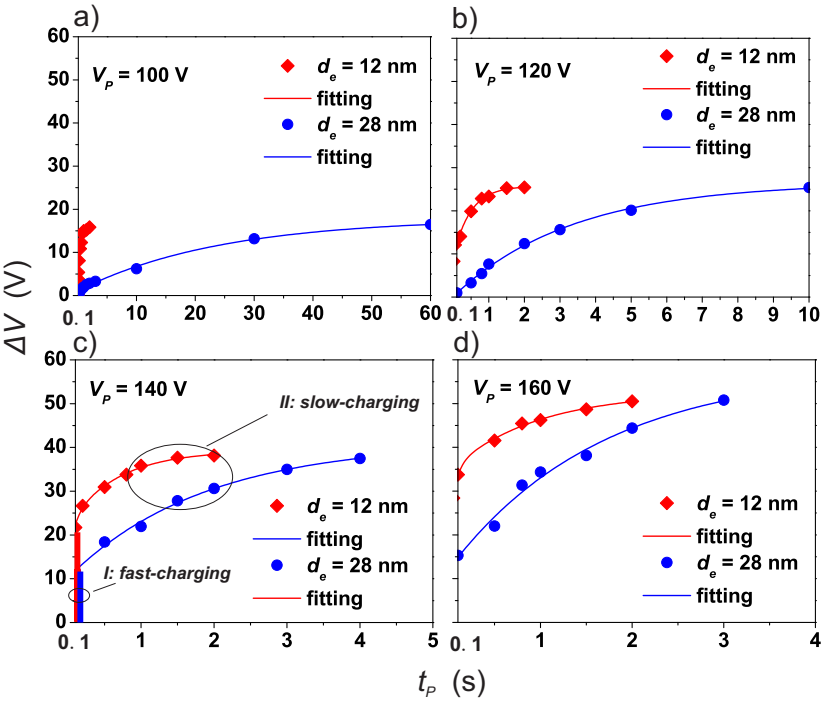


Figure 5.7. ΔV of devices with different d_e (red diamonds - d_e = 12 nm and blue points - d_e = 28 nm) over time at (a) V_P = 100 V, (b) V_P = 120 V, (c) V_P = 140 V, and (d) V_P = 160 V.

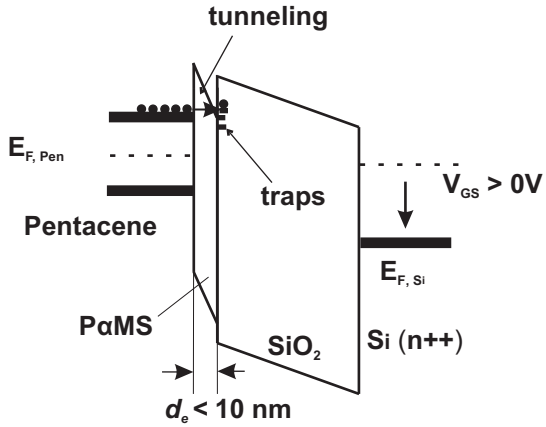


Figure 5.8. Scheme of energy bands during the programming process with a positive voltage in case of a thin electret.

In contrast, for a thick electret film ($d_e > 10$ nm), the situation becomes more complicated. If E_e is very high, it is comparable to the case of a thin electret, in which electrons gain enough energy to tunnel through. However, for moderate E_e, the carrier transport is now affected by material properties of the electret, including the trap density and energy levels of traps. Carrier transport in the thick electret can be treated as a two-step transport, as shown in Fig. 5.9. There is no enough energy for electrons to pass through the electret directly, instead getting easily captured by trap states near the interface energy barrier after a tunneling process. If the E_e lasts, the trapped electrons can be promoted from the traps into the conduction band. However, they may soon be recaptured in the next nearby vacant traps before they get accelerated by E_e. The left empty traps will be instantly refilled by newly tunneled electrons. In this way, electrons migrate through the electret by hopping among the inner trap states. The characteristic time (1 s to 10^2 s) of this transport is much longer than that of a tunneling process [138]. Thus, it is also called the slow-charging process of an ONVM cell, which is terminated when E_e becomes smaller than E_{e0}.

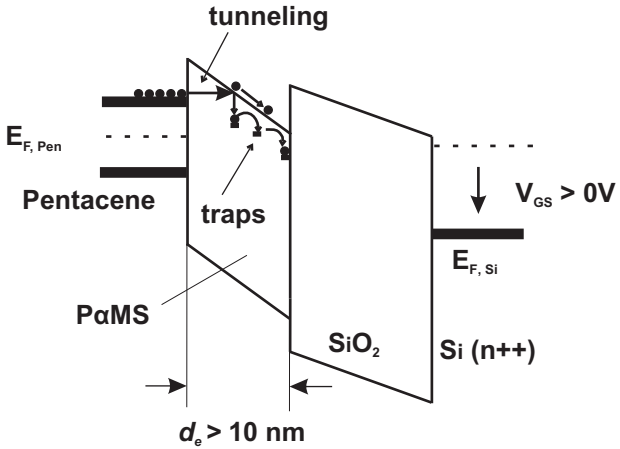


Figure 5.9. Scheme for energy band diagrams during the programming process with a positive voltage in case of a thick electret.

Interpretation of the measurement results

In this work, since d_e of all tested devices are thicker than 10 nm, the transport mechanism in thick electrets should be used to interpret the measurement results.

E_e can be calculated by [38]:

$$E_e = \frac{V_P}{d_e + d_{ox}\frac{\epsilon_1}{\epsilon_2}} + \frac{Q/\sigma}{\epsilon_1 + \epsilon_2 \frac{d_e}{d_{ox}}} \tag{5.2}$$

where d_{ox} is the thickness of the gate dielectric (SiO_2), ϵ_1 and ϵ_2 are permittivities of PαMS and SiO_2, respectively, and σ is the active area of injected currents. At $t_P = 0$, a V_P is applied on the gate of an ONVM cell, no charges have been stored yet($Q = 0$), and thus E_e has its maximal value $E_{e,max}$. If $E_{e,max}$ is so high that electrons gain comparable energy to trap states in the electret, they can penetrate the electret without getting trapped and directly reach the PαMS/SiO_2 interface. This refers to a fast-charging process, which forms the abrupt increase of ΔV appearing at $t_P = 0.1$ s in Fig. 5.7(b)-(d) (indicated as I in Fig. 5.7(c)). According to Eq. 5.2, $E_{e,max}$ for the device with a 12-nm-thick PαMS layer are 4.2, 5.1, 5.9, and 6.7 MV/cm for V_P of 100, 120, 140, and 160 V, respectively, whereas $E_{e,max}$ for the device with a 28-nm-thick PαMS layer are 3.9, 4.7, 5.5, and 6.3 MV/cm for the same values of V_P. We can

see that the abrupt increase of ΔV emerges in both devices only when $E_{e,max}$ exceeds 5.0 MV/cm.

If $E_{e,max}$ is relatively low or when E_e is reduced to moderate values due to the reverse internal electric field built by Q (both are still higher than E_{e0}), a slow-charging process occurs. Injected electrons slowly migrate along the route of trap-conduction band-trap, and eventually reach the PαMS/SiO_2 interface after a time, depending on the amount of trap states in the PαMS film. The slow growths of the curves in Fig. 5.7(a)-(d) (specially indicated by II in Fig. 5.7(c)) exhibit such slow-charging processes of the ONVM devices. We can see that the charging process in the device with $d_e = 12$ nm is faster than that in the device with $d_e = 28$ nm (red curves v. blue curves in Fig. 5.7(a)-(d)). This is because more trap states in the thick electret result in a slower transport of electrons, with the assumption that the distribution of traps in the PαMS layer is uniform.

During the programming process, E_e consistently declines due to increasing numbers of stored electrons through the charging process. When E_e becomes lower than the critical value E_{e0}, no electrons can be injected into the PαMS layer anymore, and thus the slow-charging process ceases. Consequently, the stored charge approximates to a saturated value Q_{max}. Since d_{ox} is much thicker than d_e for all devices in this study and E_{e0} is solely dependent on the energy barrier between pentacene and PαMS, Q_{max} can be treated as the same for devices with different d_e under the same V_P. This gives the reason for the convergent final values of ΔV in each subplot of Fig. 5.7. However, under the same conditions of t_P and V_P, the memory cell with a thin electret layer can be charged faster than the one with a thick electret, and thus obtains a higher ΔV. In other words, the shift of the $\Delta V = f(V_P)$ curves in Fig. 5.5 is caused by insufficient charging of devices with large d_e within the programming time of 1 s.

Finally, we come to the concept of programming efficiency that was mentioned in Sec. 5.1.3. In comparison with a thick-electret ONVM cell, a thin-electret ONVM cell can achieve a certain ΔV either under a lower V_P within the same t_P or within a shorter t_P under the same V_P. Hence, it can be concluded that devices with thinner electret films possess higher programming efficiency.

5.3.2 Characterization of Charge Retention Property

In the presented ONVM structure, the electret film also functions as a blocking layer that prevents the loss of stored charge. The thickness of the electret d_e

affects the charge retention property of ONVM cells due to its impact on the back tunneling of stored electrons. The influences of d_e on the charge retention property are investigated in this subsection.

Three representative devices with the d_e of 12, 28, and 45 nm are selected for comparison. Retention characterization is undertaken according to the protocol described in Sec. 3.2.3. Output currents of each device after the programming and erasing processes are measured, separately. t_P is fixed at 1 s for each measurement, whereas V_P is chosen differently for devices with different d_e, namely 100 V for d_e = 12 nm, 140 V for d_e = 28 nm, and 160 V for d_e = 45 nm. This setup is aimed at obtaining the same ΔV of about 15 V within the t_P of 1 second among the devices for a more straightforward comparison, as seen in Fig. 5.5.

The measured results of devices with thin (12 nm) and thick (28 nm, 45 nm) electret films are demonstrated in Fig. 5.10(a)-(c), respectively. We can see that all devices show good charge retention properties, where memory ON/OFF ratios are larger than 10^4 after 10^3 s. Particularly, we can see that the speed of the discharge behavior of the current curve decreases with increasing d_e. The leakage of the stored electrons is the critical process that results in the discharge of the current curve. In order to discuss the discharging processes of the ONVM devices, the change of "ON" current in each device was analyzed.

For a better understanding of decay behavior of "ON" currents in different devices, the measured $|I_{DS}|$ curves can be fitted by an exponential decay function according to Ref. [139]:

$$I = I_0 + I_1 \exp(-t/t_1) + I_2 \exp(-t/t_2) + I_3 \exp(-t/t_3) \tag{5.3}$$

with the time constants t_1, t_2, and t_3. By comparing the fitting results in Fig. 5.11, we can see that t_1 in all devices is approx. 8 s, and values of t_2 are in the range of 70–80 s, both showing little dependence on d_e. In contrast, values of time constants t_3 are much larger and clearly increase with d_e. Specifically, we have t_3 = 604 s for d_e = 12 nm, t_3 = 761 s for d_e = 28 nm, and t_3 = 833 s for d_e = 45 nm.

As discussed in [139], different time constants correspond to different energy levels of trap states in the electret. For instance, the so-called shallow trap states located near the conduction band are reflected by short time constants, as electrons trapped in shallow traps can be easily released after V_P is removed [140]. Since energy levels of shallow traps are mainly determined by intrinsic material properties of the electret and its surface conditions, the corresponding

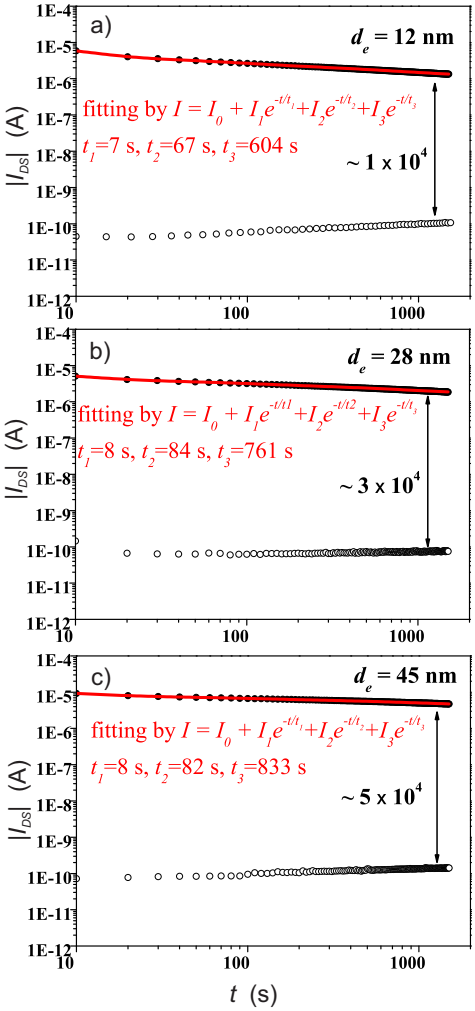


Figure 5.10. Retention characteristics of memory devices with (a) d_e = 12 nm (b) d_e = 28 nm (c) d_e = 45 nm. Output currents were measured at saturation region (V_{DS} = -60 V, V_{GS} = -10 V). The red lines are exponential fitting functions.

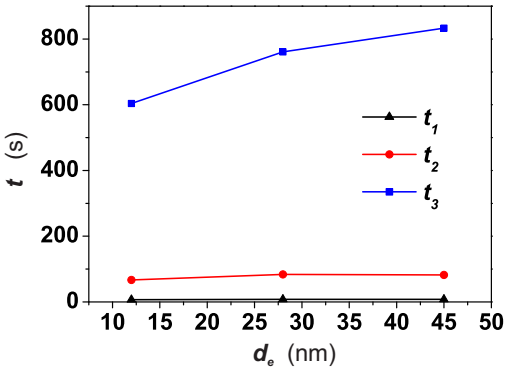


Figure 5.11. Time constants of the fitting functions for ONVM devices with different electret thickness d_e.

time constants should be hardly changed by d_e. This is a reason for the observed small changes in t_1 and t_2. Due to their weak trapping effect, shallow traps are usually not regarded as the main trapping sites of ONVM cells.

In contrast, electrons that mainly contribute to memory behavior of an ONVM cell are stored deeply in the PαMS layer or at the PαMS/SiO_2 interface. The release of the stored charge there is much slower. The time constant t_3 corresponds to this slow-releasing process and thus is indicative of the charge retention property of the memory cell. Considering that the SiO_2 layer is too thick to tunnel through, the releasing path for stored electrons is believed to be the route through the PαMS film, as shown in Fig. 5.12. After V_P is removed, trapped electrons form a reverse electric field across the PαMS film. This electric field can lead to back tunneling of the electrons – an opposite two-step transport of what happens during the programming process. Hence, the conclusion in Sec. 5.3.1 can be used here to interpret the results. That is, leakage current decreases with increasing d_e, because a thick electret film has more trap states that hinder the back tunneling of stored electrons. That is why t_3 increases with d_e in the results. In other words, increasing d_e can improve the charge retention property of a charge-trapping ONVM device. But this improvement on charge retention property sacrifices programming efficiency of the ONVM device.

In summary, the fabricated ONVM cells have potential to be an attractive application of OFETs, but the device performance of the ONVM cells in this

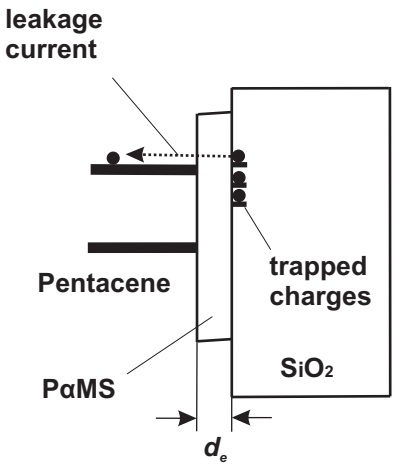


Figure 5.12. Schemes for the energy band diagrams after V_P is removed.

study is still very weak. OFETs fabricated on Si substrates with a thick SiO_2 film of 300 nm have very large operating voltages (> 60 V) and programming voltages (> 100 V). For an integrated circuit or a compact electronic system, such high voltages can cause large power consumption, worsen the problem of heat dissipation, and damage the circuit permanently. To reduce the high operating voltages, one of the most effective strategies is to increase the gate capacitance by downsizing the gate dielectric. Furthermore, the thickness of the electret layer was observed to play a crucial role in the programming efficiency of an ONVM cell. In order to increase programming efficiency, the thickness of the electret layer is desired to be further reduced. However, the tradeoff between programming efficiency and charge retention property has to be balanced during the optimization.

Chapter 6

Optimization of Charge-Trapping ONVM Cells

This chapter starts with a brief literature overview of previous efforts towards optimization of charge-trapping ONVMs. In Sec. 6.2, thin SiO_2 substrates are applied for the fabrication of OFET-based ONVMs with two types of electret structures: single-layer and bilayer electrets. The results show that the fabricated OFETs can be operated at low voltages and have relatively high field-effect mobilities. Moreover, memory properties, including programming efficiency, charge retention property and endurance behavior, are all improved in the device with a bilayer electret.

Parts of the results in this chapter have been published in Ref. [141].

6.1 A Literature Overview of the Optimization of Charge-Trapping ONVMs

Targets of the optimization of charge-trapping ONVM cells include the following aspects:

- Memory window, which is influenced by the amount of trapping sites in the gate dielectric, should be increased to improve the storage capability of charge-trapping ONVM cells.

- Charge retention property and endurance behavior of charge-trapping ONVM cells need to be improved. For example, commercial flash memories nor-

mally have a retention time of more than 10 years and can be written and erased for more than 10^6 P/E cycles.

- Operating voltages and programming voltage of charge-trapping ONVM cells have to be lowered. For example, current commercial flash memories are operated in the range of 15-17 V [142].

Early strategies to optimize charge-trapping ONVMs focusing on electret materials, for example, can be found in works of Baeg *et al.* in 2006. They firstly reported high performance nonvolatile memory devices based on OFETs with an extra polymeric gate dielectric layer of PαMS [70]. In the works [71, 143], they investigated the influence of the polarity of polymers on memory performance. By comparing memory characteristics of OFETs with different polymeric electrets, they came to the conclusion that non-polar polymers, such as PαMS, PVN or PS, could induce larger memory windows than polar polymers, such as PVA, polyvinylpyrrolidone (PVP) or polyvinylpyridine (PVPyr). However, the physical mechanisms behind this conclusion were not clear at that time.

From 2012 to 2013, Dao *et al.* fabricated n-type ONVM transistors based on fullerene and p-type ONVM transistors based on pentacene by using the same polymer of poly(perfluoroalkenyl vinyl ether) (CYTOP) as electret. In the papers [36, 107], they discussed possible positions of trapped charges by using different device configurations, such as ITO/CYTOP/pentance/Au, Si (n++)/CYTOP/C_{60}/Au, and Si (n++)/SiO_2/CYTOP/pentacene/Au. They found that memory behavior was only observed in devices with double insulating layers of CYTOP and SiO_2. Therefore, they concluded that injected charge carriers were trapped at the interface between electret and gate dielectric.

In fact, the position of stored charge carriers largely depends on the thickness of the electret. According to the report from Ref. [38] and the results in Chapter 5, it is believed that part of the injected charges can be captured in the electret when the thickness of the electret increases. However, a thick electret cannot enlarge the memory window of an ONVM cell, because the increased thickness of the electret also impedes the tunneling of charge carriers. In other words, the non-polar electret behaves more like a tunneling layer rather than a trapping layer in charge-trapping ONVMs. Although decreasing the electret thickness is an effective strategy to reduce the programming voltage of charge-trapping ONVM cells, the charge retention property of the memory cells will be worsened due to easier back tunneling of stored charge carriers as a consequence.

Therefore, by merely changing the electret material or adjusting the thickness of the electret, it is difficult to achieve a balanced optimization.

Recently, some novel ideas have emerged with the advancement of manufacturing technologies. For example, Lee *et al.* reported charge-trapping ONVM devices with molecular-scale charge-trapping centers in a PMMA electret [144]. Those embedded small molecules contained triphenylene cores with either hydroxyl or methoxyl end groups, which are well-known effective electron traps. The thickness of PMMA was approx. 10 nm, which allowed a relatively low programming voltage of 40 V to obtain a memory window of 20 V. Similar work was done by Yi *et al.*, who utilized a porous structure of PMMA to enhance the trapping effect of nonvolatile memories [129]. Furthermore, the work from Shi *et al.* has reported a high performance nonvolatile memory device by using nanofibrous electret arrays embedded in a PS layer [105]. There are many other similar proposals, such as [41], [105], [145], [146], [147] or [148]. They are mostly based on the same principle, which improves memory performance by inserting extra discrete trapping sites without changing chemical properties of gate dielectric surfaces. Even though some of the devices have achieved better results, complicated preparation processes for those electret structures contradict the original intention of easy manufacturing for charge-trapping ONVMs.

Alternatively, the idea of inserting a continual charge-trapping layer (CTL) that contains numerous trap states came into view. This trapping layer can be sandwiched between the gate dielectric and a non-polar electret layer that functions as the tunneling layer. The solution-based deposition of the extra CTL is simple and well compatible with the fabrication of OFETs. One of the earliest works based on this strategy was published by Park *et al.* in 2012 [149]. This research group fabricated charge-trapping ONVMs with a bilayer electret by using graphene oxide as the charge storage layer and PMMA as the tunneling layer. The fabricated ONVM devices exhibited a field-effect mobility of 0.1 cm^2/Vs and a memory window of 24 V under a programming voltage of 80 V kept for 10 s. Although this work realized the idea of a bi-electret structure and improved device performance at that time, high operating voltages and long programming time are clear drawbacks. In 2017, Xu *et al.* reported a low-voltage charge-trapping ONVM with a bi-electret structure of PαMS and HfO_2. This memory device could be operated at a low voltage of 8 V and showed excellent memory properties, including impressive data retention (ON/OFF current ratio of 10^4 after 10^4 s), good endurance (more than 2000 P/E cycles), and a short

programming time of less than 10 ms. However, the trapping layer HfO_2 is an inorganic material that cannot be prepared by solution-based processes. Using a combination of organic materials as the bilayer electret for the fabrication of ONVMs therefore remains of high interest.

PVA is a commonly seen polar polymer that shows high charge-trapping effects owing to its abundant hydroxyl groups [150–152]. Moreover, PVA is dissolved in water, and thus the preparation of a PVA trapping layer can be easily realized by using a spin-coating process. If a PVA layer is applied alone as the electret in a charge-trapping ONVM device, the high polarity of the PVA layer can lead to poor field-effect mobilities, as shown in Sec. 4.2 and in Ref. [109]. This is because the polar dielectric induces broader energetic disorder of electronic localized states at the semiconductor surface, which impedes the charge transport and lowers the field-effect mobility of an OFET [153–155]. However, if the PVA layer is used as a trapping layer in a bi-electret structure, the polar surface of PVA can be covered by a non-polar tunneling layer, whereas the rich trapping sites provided by PVA will not be influenced. The device performance of the fabricated ONVM cell is thus supposed to be improved.

In this chapter, ONVM cell optimization adopts the idea of a bilayer electret structure by using the organic material combination of PαMS and PVA. Measurement results and discussions for the underlying physical mechanism will be demonstrated in the following section.

6.2 Low-Voltage ONVMs with Single-Layer and Bilayer Electrets

In this section, low-voltage charge-trapping ONVM devices with single-layer and bilayer electrets are fabricated. PαMS is used as the tunneling layer, while PVA is adopted as the CTL for the bi-electret devices. Electrical properties of the ONVM cells are investigated, including field-effect mobilities, threshold voltages, memory windows, charge retention property, and endurance behavior. At the end, the understanding of the memory mechanism in bi-electret charge-trapping ONVMs will be discussed.

6.2.1 Thin SiO_2 Substrates

The use of thick Si substrates with a 300-nm SiO_2 film was mainly considered for a stable fabrication early on in the research project. For practical application

however, operating voltages, which are more than 60 V for the devices discussed in former chapters, must be reduced. The easiest strategy to reduce the operating voltages is to increase the capacitance of the gate dielectric C_i' by utilizing a thinner SiO_2 film as the gate dielectric due to its reliable insulating property and easy commercial availability. In this chapter, deeply n-doped Si wafers with a 50-nm-thick SiO_2 film purchased from *Silicon Materials GmbH* are used for the fabrication of low-voltage ONVM cells.

6.2.2 Experimental

Schematic structures of OFETs with single-layer and bilayer electrets are illustrated in Fig. 6.1(a) and (b), respectively. The thickness of PαMS is marked as d_t and the thickness of PVA is labeled as d_c. Organic materials for the fabrication of ONVM transistors, including PαMS ($M_n \sim 427{,}000$), PVA ($M_n \sim 89{,}000$ – 98,000, > 99% hydrolyzed), and pentacene (sublimed grad > 99.9%, HOMO ~ 5 eV, LUMO ~ 3 eV), were purchased from *Merck KGaA*. As preparation, solid PαMS powder was dissolved in toluene to make PαMS solutions, with different concentrations (0.25 and 0.5 wt%). Another solution of 0.5 wt% PVA was made by mixing the PVA powder in distilled water, heated at approx. 90 °C on a hot plate. The substrates with an area of 20 × 15 mm were divided into two groups. One substrate was used to fabricate bi-electret ONVM cells, labeled as Group A, whereas two substrates were used for the fabrication of single-electret ONVM cells, labeled as Group B.

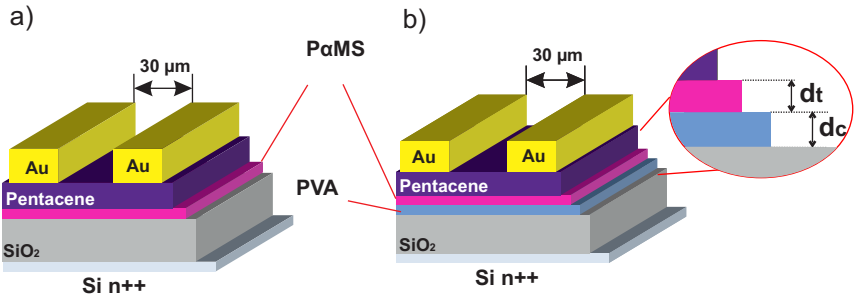


Figure 6.1. Schematics of the bottom-gate ONVM device with (a) a single electret and (b) a bi-electret structure. d_t and d_c represent the thickness of the tunneling layer PαMS and the trapping layer PVA, respectively.

First, the substrates were cleaned by the cleaning process described in Sec. 3.1. Afterwards, they were heated in a hot vacuum oven at 120 °C for more than 30 min. Then, the substrate from Group A would be coated by a PVA layer of approx. 12 nm and a PαMS layer of 6 nm via spin-coating processes, sequentially. Between subsequent coating processes, the substrate was dried in the vacuum oven for 10 min. On the other hand, the substrates from Group B would be covered by a PαMS film of 6 nm or a PαMS film of 12 nm. The thickness of the coated PαMS film was controlled by the solution concentration. The rotation speed (3000 rpm) and the rotation duration (60 s) were kept the same for each spin-coating process. Subsequently, substrates were baked in a vacuum oven for another 1 h. So far, three different configurations of the gate dielectric were obtained. The substrates of Group B had a single electret of different thicknesses ($d_t = 6$ nm or $d_t = 12$ nm), whereas the substrate of Group A was coated by a bilayer electret ($d_t = 6$ nm and $d_c = 12$ nm). Next, a pentacene layer of 30 nm was deposited on the prepared substrates in a high vacuum ($P < 10^{-6}$ mbar) chamber at a deposition rate r_p of approx. 0.5 Å/s. Finally, Au drain and source electrodes with a thickness of 40 nm were deposited through a shadow mask by a similar thermal evaporation process at a low deposition rate r_{Au} of 0.1 Å/s. Five transistors were formed on each substrate. The channel width W was 1 mm and the channel length L was 30 μm.

The morphology and surface energy of each insulating layer were investigated by an atomic force microscopy (AFM) and a drop shape analyzer (DSA), respectively. Electrical properties of the devices were characterized by measurement platforms based on the semiconductor analyzer *Agilent* 4155C/4156C.

6.2.3 Morphological Properties of the Gate Dielectric Surface

As mentioned in former chapters, surface properties of the gate dielectric, such as surface energy and surface roughness, influence electrical characteristics of OFETs. Therefore, water contact angle θ and average surface roughness R_a on different films were measured. The results are presented in Fig. 6.2.

We can see that the R_a of a SiO_2 substrate is 0.234 nm, and the spin-coating process of each film on it hardly changes R_a. This means that both the single electret and the bilayer electret provide a smooth surface for the deposition of pentacene. In contrast, it can be seen that θ of different films varies strongly. On the pristine SiO_2 substrate, θ is nearly 80° (measured after heating the substrates at 120°C in vacuum). This value is reduced to about 62° by covering the SiO_2

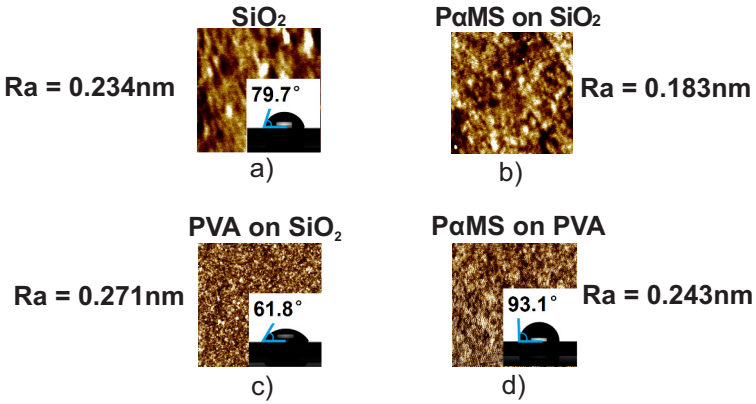


Figure 6.2. AFM morphological graphics and contact angles of (a) SiO_2, (b) PαMS on SiO_2, (c) PVA on SiO_2, and (d) PαMS on PVA. The AFM diagrams were measured by scanning the surface in an area of 2 × 2 μm.

surface with a PVA film, whereas the covering of a PαMS layer on the PVA surface increases θ to more than 90°. It is well known that a big contact angle on the surface reflects a low surface energy, which can facilitate the pentacene film formation during the deposition. A well-ordered pentacene film supports the transport of charge carriers and thus contributes to a large field-effect mobility of the transistor. Since the non-polar PαMS layer is applied as the interface to pentacene in both types of ONVM cells, they should have comparable field-effect mobilities.

6.2.4 Electrical Properties of the OFETs

Output curves and transfer curves of the OFETs with different gate dielectrics were measured by the measurement platform mentioned in Sec. 3.2.2. The results are illustrated in Fig. 6.3, Fig 6.4, and Fig. 6.5.

We can see that operating voltages of the fabricated OFETs are significantly reduced in comparison to the values for OFETs fabricated on substrates with a thick SiO_2 film. In particular, as shown in Fig. 6.4 and Fig. 6.5, when voltages of V_{GS} and V_{DS} are lowered down to -12 V, transistors with $d_t = 6$ nm can still achieve output currents of more than 6 μA. To achieve a comparable value in OFETs fabricated on substrates with a 300-nm thick SiO_2 as the gate dielectric, the applied voltages has to be five times higher. Besides, d_t shows an impact on

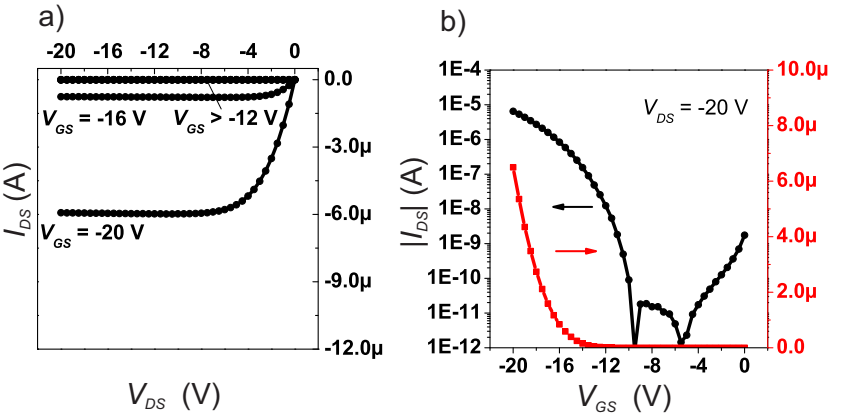


Figure 6.3. (a) Output and (b) transfer curves of the OFET with a 12-nm-thick PαMS. In (b), the red line shows the results in the linear-scaled y-axis (right), and the black line shows the results in the logarithmic-scaled y-axis (left).

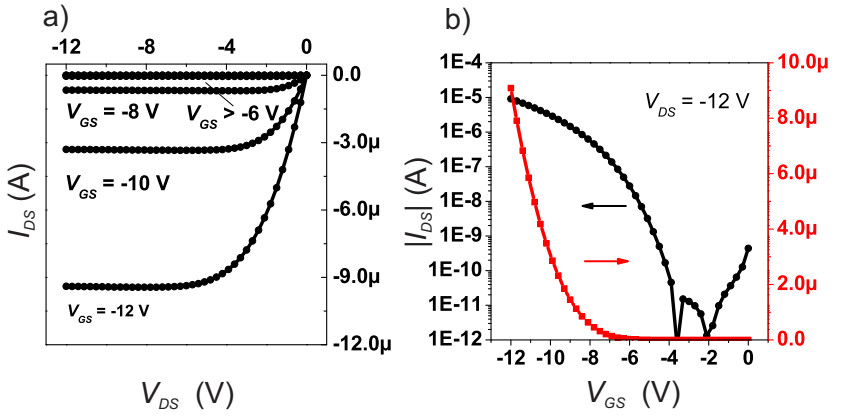


Figure 6.4. (a) Output and (b) transfer curves of the OFET with a 6-nm-thick PαMS. In (b), the red line shows the results in the linear-scaled y-axis (right), and the black line shows the results in the logarithmic-scaled y-axis (left).

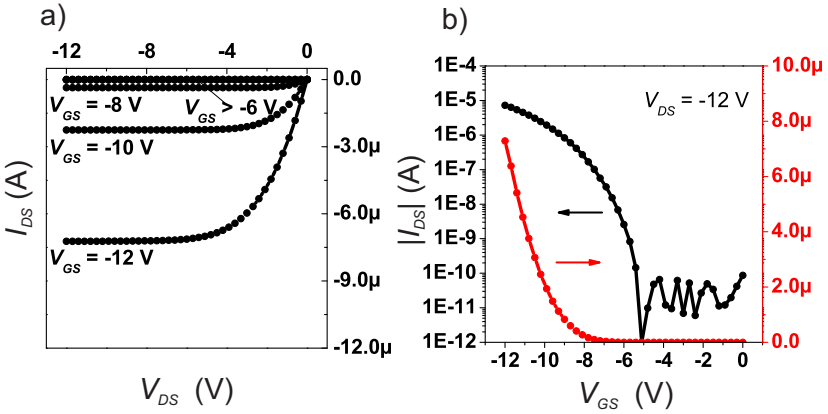


Figure 6.5. (a) Output and (b) transfer curves of the OFET with a bilayer electret containing a PVA layer of 12 nm and a PαMS layer of 6 nm. In (b), the red line shows the results in the linear-scaled y-axis (right), and the black line shows the results in the logarithmic-scaled y-axis (left).

the operating voltages. In order to obtain an output current in the same range, the OFET with $d_t = 12$ nm has to be operated by V_{GS} and V_{DS} with absolute values of 20 V, which are 8 V larger than the ones of the OFETs with $d_t = 6$ nm. One possible reason for this is that the impact of the low-k PαMS layer on the capacitance of the gate dielectric cannot be neglected when its thickness is approaching the thickness of the SiO_2 film. On the contrary, the influence from the water-solution grown PVA thin film is very small due to its high dielectric constant in the form of hydrogel [156, 157].

Furthermore, transfer curves are used to extract field-effect mobilities μ_e and threshold voltages V_{th} of the OFETs. The results are summarized in Table. 6.1. It can be seen that μ_e of transistors are comparable and range from 0.3 to 0.5 cm^2/Vs, whereas V_{th} shows a difference. For example, the devices with thinner PαMS layers exhibit threshold voltages of -7.4 V and -7.6 V. These are almost half of the one with a thicker PαMS layer. The results indicate that μ_e is mainly influenced by surface properties of the gate dielectric, including surface energy and surface roughness, which are rarely changed in the OFETs with the same tunneling layer material, whereas V_{th} is impacted by the thickness of the tunneling layer d_t. Moreover, the insertion of the extra charge-trapping

Table 6.1. Electrical characteristics of OFETs with different gate dielectrics on 50 nm SiO_2 substrates

Samples	maximal V_{GS}, V_{DS} (V)	μ_e ($cm^2 \cdot V^{-1} s^{-1}$)	V_{th} (V)
12nm PαMS (single electret)	-20	0.3	-13.6
6nm PαMS (single electret)	-12	0.5	-7.4
6nm PαMS + 12nm PVA (bilayer electret)	-12	0.5	-7.6

layer mostly retains electrical properties of OFETs, including operating voltages, field-effect mobility, and threshold voltage.

6.2.5 Memory Window

The memory window ΔV, which indicates the storage ability of an ONVM cell, is defined as the width of the shift in transfer curve caused by a gate bias. The estimation of ΔV is realized by measuring transfer curves of the memory device in the programmed state and in the erased state, respectively. The concrete measurement procedure and the measurement platform are described in Sec. 3.2.3. It should be noted that devices with different thicknesses of the tunneling layer d_t were measured by distinct ranges of V_P, because there might be no memory effect in the device with a thick d_t if V_P is too low, whereas the device with a thin d_t might be damaged if V_P is too high. Specifically, following setups were utilized for the measurements: V_P varied from 25 V to 45 V for the device with $d_t = 12$ nm, and from 20 V to 30 V for devices with $d_t = 6$ nm. The programming time t_P was uniformly set as 1 s, which is a moderate value that is widely used for the ΔV test of ONVMs in the community.

The results show that different devices have different widths of transfer curve shifts at a fixed V_P. For example, the transfer curve shift of each transistor at $V_P = 30$ V is illustrated in Fig. 6.6(a)-(c). ΔV is estimated by the difference between the turn-on voltage V_{on} of the transfer curve after the programming process and the one after the erasing process, namely $\Delta V = |V_{on+} - V_{on-}|$, where V_{on} is defined as the gate voltage, at which the output current I_{DS} first reaches 100 pA after the transistor turns on. Besides, since injected electrons

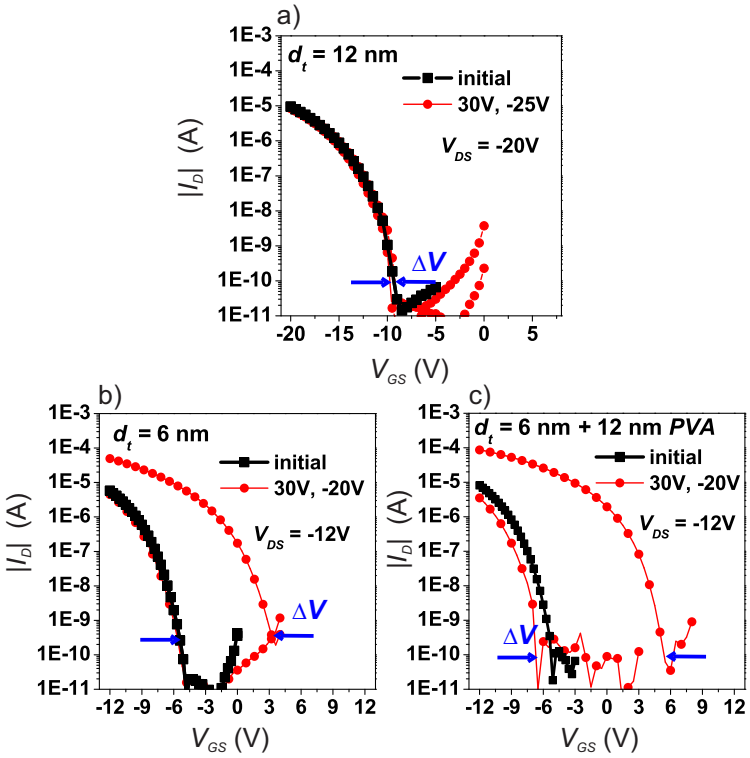


Figure 6.6. Shifts of transfer curves after programming/erasing of the transistor with (a) a single electret of 12-nm-thick PαMS, (b) a single electret of 6-nm-thick PαMS, and (c) a bilayer electret containing a PαMS layer of 6 nm and a PVA layer of 12 nm.

are mostly stored in the trap states underneath the electret according to [36], the density of captured charge carriers can be roughly estimated by [144] [158]:

$$\Delta n = \frac{\Delta V}{q} \cdot C'_{ox} \tag{6.1}$$

where q is the elementary charge and C'_{ox} is the capacitance per unit area of the oxide. The results in Table 6.2 show that memory cells with d_t = 6 nm show larger ΔV and higher density of trapped electrons, whereas the device with d_t = 12 nm demonstrates a very small ΔV, which means that the V_P of 30 V is insufficient to write information into this memory cell. Particularly, the device with a bi-electret structure achieved a ΔV of 12 V, 30% larger than the value of its counterpart with a single electret.

Table 6.2. Memory windows and the density of stored electrons in ONVM devices with different types of electret

Samples	ΔV at V_P = 30 V (V)	Δn at V_P = 30 V (cm^{-2})
12nm PαMS (single electret)	0.5	2.1×10^{11}
6nm PαMS (single electret)	8.7	3.6×10^{12}
6nm PαMS + 12nm PVA (bilayer electret)	12.0	5.0×10^{12}

Furthermore, memory windows of devices with single-layer and bilayer electrets are compared in relation with V_P ranging from 18 V to 40 V in Fig. 6.7. It can be seen that ΔV increases with increasing V_P in three devices for a fixed t_P. To obtain the same ΔV as the other devices, the device with d_t = 12 nm, however, requires a higher V_P. This result implies that one can reduce the programming voltage of a memory cell by reducing the thickness of the tunneling layer. On the other hand, we can see that the device with an extra PVA film has a larger ΔV than the device with a single electret when they are programmed by the same V_P. This result confirms that the insertion of the PVA film enhances the storage ability of the memory device. The reason for this enhancement is that the large amount of introduced trap states in the PVA film improves the

trapping probability of charge carriers after they pass through the tunneling layer.

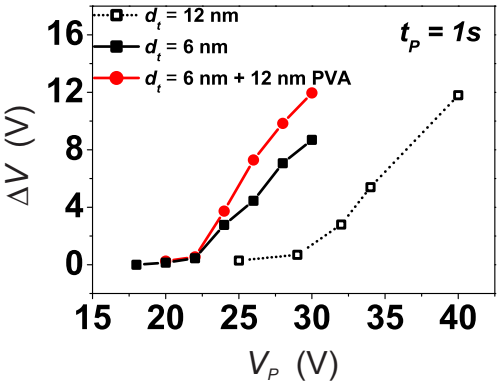


Figure 6.7. ΔV of devices with different electret structures within a programming time $t_P = 1$ s related to programming voltage V_P. © 2019 IEEE.

6.2.6 Programming Dynamics

To investigate the programming dynamics of the memory cells, ΔV of devices with single electrets ($d_t = 6$ nm and 12 nm) for varied t_P were measured as the first investigation step. V_P was chosen as 30 V, which is close to the critical V_P for the device with $d_t = 12$ nm to show memory behavior. The results are shown as the black solid and dotted curves with boxes in Fig. 6.8. One can see that, compared to the device with $d_t = 12$ nm, the device with $d_t = 6$ nm requires a two orders of magnitude shorter programming time t_P to obtain the same ΔV. Afterwards, the same measurement was undertaken in the bi-electret ONVM cell. Within the same short t_P of 0.2 s, the bi-electret ONVM cell can obtain a ΔV of 9 V, which is even larger than the device with a single-layer electret of 6 nm, as the red curve shows in Fig. 6.8. The reason behind this result has been discussed in Chapter 5. For a relatively thick tunneling layer, charge carriers cannot directly tunnel through it and move via a relatively slow two-step transport process, which is mainly influenced by trap states that exist in the tunneling layer. By downsizing d_t, the number of the trap states in the transport path is reduced, assuming that trap states in the tunneling layer are uniformly distributed. This reduces the occurrence of the two-step transport

process, and charge carriers mainly move through the ultrathin electret via a fast tunneling process. Since the time of the tunneling process is much shorter than the two-step transport process, the programming speed is thus increased.

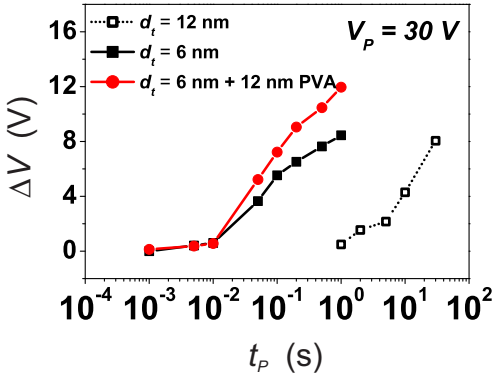


Figure 6.8. ΔV of devices with different electret structures under the programming voltage V_P = 30 V related to programming time t_P. © 2019 IEEE.

6.2.7 Charge Retention Property

In nonvolatile memories, there are discharging processes which lead to a loss of information after a certain time [159, 160], the so-called retention time. In ONVMs, one usually evaluates the charge retention property of an ONVM by observing the ON/OFF current ratio after a long measurement time. In this work, the retention performance of the memory cells with single-layer and bilayer electrets were separately characterized, where the measurement procedure is as follows. In the first step, the device under test was initialized by five repeated cycles of program/erase (P/E) to obtain a stable initial state. In the second step, a program signal was applied to set the device into the state "ON". Finally, the output current at the drain electrode I_D, which is labeled as the "ON" current, was measured for 10^4 s. The concrete method for the measurement of I_D over time can be seen in Sec. 3.2.3. For the measurement of the "OFF" current, the device was also firstly initialized. Then, the output current I_D in the state of "OFF" was measured with the same set of read voltages. Voltages for measurements of devices with different d_t were varied (V_{GS} = -8 V, V_{DS} =

-20 V for d_t = 12 nm, and V_{GS} = -4 V, V_{DS} = -12 V for d_t = 6 nm). The different setup is used to adjust output currents of the devices so that they are in the same region for a straightforward comparison.

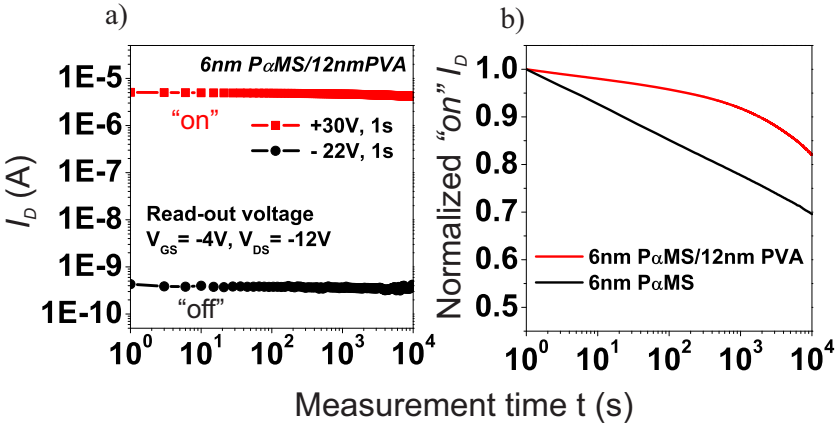


Figure 6.9. (a) Retention characteristics of the device with an electret structure of 6 nm PαMS/12 nm PVA. (b) Normalized "ON" currents of devices with single- and bilayer electrets relative to linear scaled time.© 2019 IEEE.

In Fig. 6.9(a), measurement results of the device with the bilayer electret are demonstrated in a coordinate system with double-logarithmic axes. We can see that this device has a relatively high ON/OFF ratio of more than 10^4 after a time of 10^4 s. Fig. 6.9(b) shows the normalized "ON" currents of the single-electret and the bi-electret device relative to linear scaled time. It can be seen that the device with an additional PVA film demonstrates a slower reduction of I_D than the device with the single electret. Particularly, it can be seen that there is a loss of about 7% at 10 s after the programming process in the device with the single electret, whereas this effect is significantly reduced in the device with an extra PVA film (only about 2%). Furthermore, at 10^4 s after the programming process, the I_D in the device with the single electret is reduced to less than 70% of the initial current, whereas the device with the bi-electret is still able to deliver more than 80% of its initial current. As mentioned in Chapter 5 and in other reports [161], [129], and [148], reducing d_t is a tradeoff between programming

efficiency and charge retention property in devices with single electrets. Here, this problem can be relieved by inserting an extra charge-trapping layer of PVA.

6.2.8 Endurance Behavior

As defined in Sec. 2.2.1, endurance behavior of nonvolatile memory cells is indicated by its maximum bearable P/E cycles. Endurance behavior of single- and bi-electret devices with a 6-nm-thick tunneling layer were characterized by measuring "ON" and "OFF" currents after each programming and each erasing process. Details for the measurement procedure can be found in Sec. 3.2.3. The results are demonstrated in Fig. 6.10. We see that the bi-electret device can retain two distinct current states with an ON/OFF ratio of approx. 10^4 after more than 500 P/E cycles, whereas the ON/OFF ratio of the device with a single electret became continually smaller with increasing numbers of P/E cycles. The device with the bi-electret structure has clearly better endurance behavior than its counterpart with the single electret.

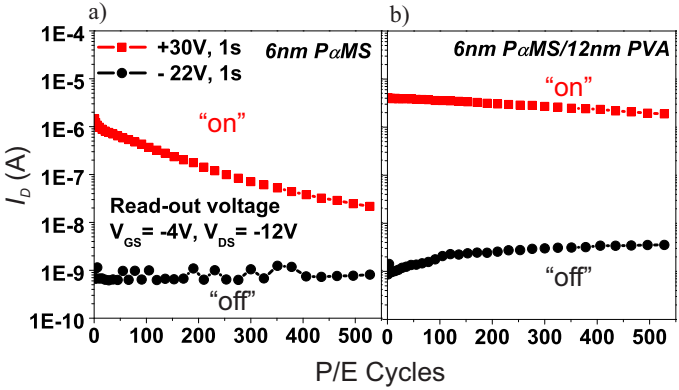


Figure 6.10. Endurance characteristics of devices with electret structures of (a) 6 nm PαMS and (b) 6 nm PαMS/12 nm PVA. © 2019 IEEE.

6.2.9 Description of the Memory Mechanism

In order to understand the functionality of the inserted PVA layer, the work mechanism of this memory structure should be taken into account.

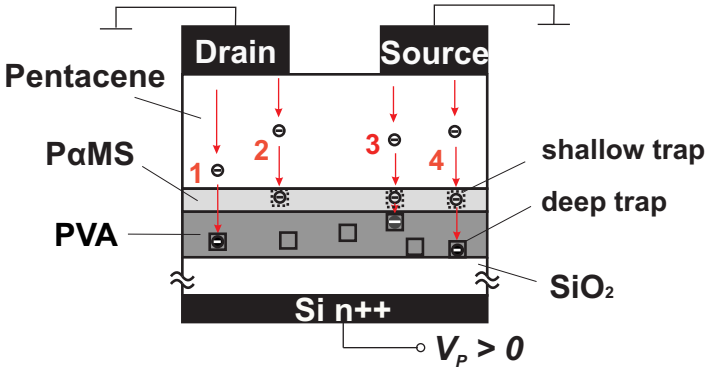


Figure 6.11. Schematics of the mechanism of the device with double electrets during the programming process. The red numbers from 1 to 4 describe different mechanisms of the carrier transport.

During the programming process, a programming voltage V_P is applied at the bottom gate, and the source and drain electrodes are connected to ground, as shown in Fig. 6.11. Electrons are injected from the electrodes and move towards the direction of the gate. Depending on the energy and the amount of trap states that electrons encounter along the transport path, the electrons will reach different depths of the electret [162]. Electrons with high energy can directly tunnel through the PαMS layer [163] and get trapped in the PVA film, shown as process 1 in Fig. 6.11. Electrons that gain less energy can get trapped by shallow traps in the tunneling layer just after they pass through the pentacene film, shown as process 2 in Fig. 6.11. Process 1 and Process 2 belong to the one-step tunneling process, which occurs in a very short time. The injection depth of the electrons is strongly affected by d_t and V_P. On the other hand, if V_P is held for longer, some of the electrons trapped in the PαMS layer can be reactivated by the electric field and then pass through the tunneling layer via a hopping process. Eventually, the electrons arrive at the interface between the PαMS layer and the PVA layer or deeply in the PVA layer [138], illustrated as the processes 3 and 4 in Fig. 6.11. They belong to the so-called two-step transport process, which is influenced by various parameters, including the thickness of PαMS d_t, the thickness of PVA d_c, programming voltage V_P, and programming time t_P. Besides the transport processes, the number of stored electrons is also influenced by the trapping process, which depends on the density of trap states that exist between the tunneling layer and the SiO_2 layer. Induced trap

states from the PVA film increase the probability that the injected electrons get captured and thus enhance the trapping process. Therefore, the device with a reduced d_t and an extra PVA film obtained increased programming efficiency.

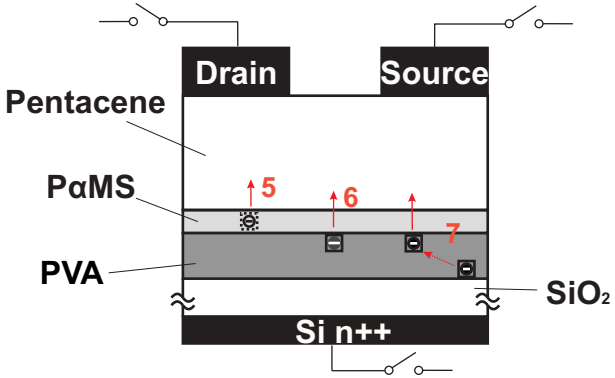


Figure 6.12. Schematics of the mechanism of the device with double electrets in retention mode. The red numbers from 5 to 7 describe different mechanisms of the carrier transport.

In retention mode, when V_P is removed, the electrons stored in different locations in the electret reveal different discharging behavior, which influence the retention characteristics of the device. The internal electric field built by the stored electrons is the main reason for the loss of the stored charge. Electrons, which get captured in the tunneling electret, will be released in a very short time due to low energy levels of shallow traps and the short leakage path (process 5 in Fig. 6.12). Hence, the effect of shallow traps on retention behavior can be neglected. Electrons stored in traps near the interface behave like the ones that are stored in the single-layer electret structure. The back tunneling process of these electrons, shown as process 6 in Fig. 6.12, mainly depends on the thickness of the PαMS layer. Increasing d_t prevents the loss of the stored charge, but also reduces programming efficiency. This gives rise to the mentioned tradeoff of d_t in the devices with single electrets. However, in the device with a bilayer electret, most electrons are captured by trap states in the PVA layer. Because of the high energy gap between the trap states and the conduction band of the insulated PVA layer, the probability that electrons move to the interface of the two polymers is considerably reduced [137], The leakage of these electrons is thus becoming more difficult, shown as process 7 in Fig. 6.12. As a result, the

charge retention property and endurance behavior in the device with the bilayer electret were enhanced.

In summary, operating voltages of the fabricated OFET-based ONVM cells are reduced down to -12 V by using substrates with a thin SiO_2 film and reducing the thickness of the tunneling layer, whereas relatively high field-effect mobilities of the transistors are retained. In addition, the device with an ultrathin PαMS layer of 6 nm and an additional PVA layer of 12 nm achieves high memory performance in two aspects. First, a large memory window of 9 V can be obtained by applying a low programming voltage of 30 V for only 0.2 s. Second, the device can retain more than 80% of its initial current after 10^4 s and keep a high ON/OFF current ratio in the magnitude of 10^4 after more than 500 P/E cycles. Therefore, the use of the bilayer electret, which is built by the organic material combination of PαMS and PVA, has successfully improved the memory performance of charge-trapping ONVM cells.

Chapter 7

Conclusion and Outlook

This dissertation has discussed electrical characteristics and a possible application of pentacene-based OFETs with modified gate dielectrics. Chemical properties of the gate dielectric surface have a strong impact on electrical properties of the transistors, such as field-effect mobility and threshold voltage. Specifically, by lowering the surface energy of gate dielectrics, field-effect mobilities of the measured OFETs are found to be increased. Furthermore, specific chemical groups on the dielectric surface can result in a charge-trapping effect, which causes a shift of the threshold voltage. By inserting a polymeric electret, which separates the semiconductor layer from the gate dielectric, the shift in transfer curve of an OFET becomes controllable even during operation. Hence, this device is regarded as a possible candidate for the realization of an ONVM cell.

In Chapter 4, two types of surface modifications were undertaken on OFET gate dielectrics. On the one hand, coating a pristine SiO_2 substrate with a polymer as a buffer layer could change its surface energy. For example, non-polar buffer layers, such as PS and PαMS, massively reduced the surface energy of SiO_2 substrates, whereas a polar buffer layer of PVA increased surface energy. By characterizing electrical properties of OFETs with different modified gate dielectrics, it was found that the field-effect mobility was improved by inserting a polymeric buffer layer, and this improvement was higher in OFETs with buffered gate dielectrics of lower surface energies. On the other hand, a UV-ozone treatment could reduce both threshold voltages and field-effect mobilities of the treated OFETs. As a compromise, applying a UV-ozone treatment on the PS-buffered gate dielectric could bring a satisfying outcome with a largely

reduced threshold voltage down to around -10 V and a reasonable field-effect mobility of about 0.2 cm^2/Vs.

There are several reasons for the observed results. First of all, the growth mode of the pentacene layer varies with the surface condition of the gate dielectric. A tight three-dimensional (3-D) arrangement of pentacene molecules can improve the interconnection and contact between adjacent pentacene grains. In this way, the pentacene thin film exhibits a higher carrier mobility. A non-polar surface or low surface energy facilitated the growth of the pentacene molecules into the 3-D molecule arrangement, so that the field-effect mobility of the OFET was increased. Furthermore, surface modification can not only change surface energy but may also introduce charge traps, which influence threshold voltages of the OFETs. For example, the applied UV-ozone treatment induced new chemical groups that have charge-trapping effects, which resulted in the shift of threshold voltages. In particular, the charge-trapping effect in gate dielectrics has laid the foundation for the application of OFETs as ONVM cells.

As a potential application of OFETs, non-volatile memory devices making use of the charge-trapping effect in gate dielectrics were fabricated and investigated in Chapter 5. A non-polar polymer PαMS was applied as the electret. ONVM cells were fabricated on deeply doped Si substrates with a SiO_2 film of 300 nm. By changing structural parameters of the devices, a change in the memory behavior could be observed. It was found that the thickness of Au electrodes in an ONVM cell had an impact on the injection of electrons. With increasing thickness of the Au electrodes the memory window of the memory cell was enlarged. Moreover, the thickness of the electret was also a crucial factor that determined not only programming efficiency but also the charge retention property of the memory device. The results showed that, by decreasing the thickness of the electret, programming efficiency of the device increased, i.e., the memory cell could achieve larger memory windows under smaller programming voltages or/and within shorter programming time, whereas the charge retention property of the device was worsened.

The results were interpreted by considering the memory mechanism of a charge-trapping ONVM cell. Stored charge carriers were injected from Au electrodes, tunneled across the electret layer and got captured in the electret or at the interface between electret and SiO_2 layer. Reducing the thickness of the electret facilitated the injection of charge carriers, resulting in higher programming efficiency. However, in retention mode, the electret layer works as a blocking

layer that prevents the leakage of stored carriers. This double functionality of the electret layer gives the reason for its contradictory behavior. In addition, in order to avoid high operating voltages, the transfer curve of the transistor is designed to shift towards positive values after a programming process. This requires the injection of electrons, which is determined by the contact between Au electrodes and pentacene layer. Increasing the thickness of the Au electrodes was found to be a possible method of improving the injection of electrons due to the changed relative positions of energy levels of pentacene and Au, and the introduced gap states at the Au/pentacene interface.

ONVM devices fabricated on thick SiO_2 substrates have shortages in device performance, including high operating voltages and low programming efficiency. In order to improve the device performance, an optimization was proposed by using thin SiO_2 substrates in Chapter 6. The fabricated ONVM cells kept relatively high field-effect mobilities of around 0.5 cm^2/Vs and could be driven by a low voltage of -12 V. The non-polar polymer PαMS was also used here to modify the gate dielectric and as a part of the electret layer. Particularly, a bilayer-electret structure was introduced to improve the memory performance of the ONVM devices. The fabricated device showed a large memory window of 9 V at a programming voltage of 30 V within a programming time of 0.2 s. The memory cell could keep a large ON/OFF current ratio of more than 10^4 for more than 10^4 s or for more than 500 P/E cycles.

In the last part of Chapter 6, the memory mechanism in bi-electret ONVM transistors was described. The main idea of this structure is to split the electret structure into a tunneling layer and a charge trapping layer. Thereby, programming efficiency is improved by downsizing the tunneling layer, whereas charge retention property and endurance behavior are retained or even enhanced by inserting the extra charge-trapping layer.

Finally, there are several possible future works which can be expanded from this dissertation. The application of OFETs should, according to views of the author, focus on applications of simple circuits, stretchable devices, special chemical sensors, and stand-alone devices, so that their advantages of low-cost and low-temperature manufacturing, mechanical flexibility, chemical endurance, and light weight can be maximally utilized. The research of OFET-based ONVMs has its worth for possible uses in the application of all-in-one chips with low storage capacity. The device performance should be further optimized in aspects of charge retention property and endurance behavior. The idea of the bi-electret

structure shows its potential for the improvement of memory behavior and electrical properties. Other combinations of non-polar and polar polymers can also be attempted. Furthermore, the charge retention behavior of ONVMs is required to be investigated in more details. A mathematical model for discharging currents in retention mode will be very helpful for the design of memory arrays.

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Cirriculum Vitae

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