Understanding and Modeling the Hysteresis in Current-Voltage (I–V) and Capacitance-Voltage (C–V) Characteristics of Organic Thin-Film Transistors

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Chapter 1

Introduction

Plastics are organic materials which are traditionally known to be good insulators. However, a discovery in 1977, which was later awarded with a Nobel Prize in chemistry, showed, the conductivity of polyacetylene, which is an organic polymer, can be modified through doping.[1] This discovery initiated new ways of using plastics in electronics as a large variety of conducting and semiconducting organic materials has been synthesized during the following years. The first transistor with an organic semiconductor was reported in 1983, which used an insoluble form of polyacetylene as the active layer.[2] However, it was not until 1988, when the first solution-based organic transistors were successfully demonstrated, that this new research area, called organic electronics, started to attract considerable interest.[3]

Solubility and low temperature processibility of organic materials turned out to be the main advantages of organic semiconductors compared to the conventional single-crystalline inorganic semiconductors, which require high processing temperatures above 800 °C.[4] Employing low-cost solution deposition techniques such as printing or casting, which take place at or slightly above room temperature, organic semiconductors can be processed on light-weight, flexible substrates which opened a new era for low-cost, foldable, large-area electronics. Over the years, the initial drawback of poor electrical performance due to the low charge carrier mobilities of early organic semiconductors has disappeared with newly synthesized organic materials and improved fabrication methods such that, today, the charge carrier mobilities of organic semiconductors outperform that of amorphous silicon, which is the state-of-the-art semiconducting material for dis-

play applications.[4,5] Consequently, the first products with organic semiconductors made their way to the shelves. Yet, with improving charge carrier mobility figures, the scientific efforts concentrated lately on instability issues, which is still a key factor that hinders the commercialization of bigger range of organic semiconductor based products.

1.1 Motivation and Aim of the Thesis

Organic transistors are known to suffer from operational instabilities in form of charge carrier mobility alterations, threshold voltage shifts, and hysteresis in the current-voltage characteristics.[4–8] Beside environmental factors such as light and humidity, intrinsic factors such as slow polarization of the gate dielectric and trap states in the semiconductor have been reported as possible causes in the literature.[9,10] However, neither the mechanisms which lead to these instabilities nor the physics behind are yet fully understood. Therefore, this thesis aims to shed light on the charge carrier trapping related instabilities of organic thin-film transistors. The main objective is to understand the physical principles which lead to hysteresis in current-voltage and capacitance-voltage characteristics. A further goal is to develop behavioral device models which reproduce, therefore make it possible to simulate, the electrical characteristics of organic transistors.

1.2 Structure of the Thesis

The present work consists of five chapters.

Chapter 2 provides a theoretical background for the rest of the thesis. It introduces the basics of charge transport in organic materials in a simple but comprehensive way. In addition to the concepts such as hybridization and conjugation, the formation of charge carriers and the charge transport in conjugated materials are explained. The second part of Chapter 2 deals with organic thin-film transistors (OTFTs). Following a brief summary about the operation principles, a detailed literature survey on organic materials used in OTFTs is presented. Moreover, OTFT fabrication techniques are reviewed and the electrical characterization measurements are explained.

In Chapter 3, instabilities of current-voltage (I–V) characteristics of OTFTs are investigated. This chapter starts with a literature review on mechanisms which have been reported to cause hysteresis in OTFTs. The next section describes the fabrication and the electrical characterization of the probes. The rest

of the chapter introduces the results of our investigations on the I–V characteristics of hybrid OTFTs. First, a theory based on hole traps is introduced to explain the observed hysteresis in the characteristics. Then, the theory is verified through device simulations. In the next section, a behavioral model of OTFTs is introduced, which can reproduce both static and transient I–V characteristics. The next section of the chapter emphasizes the difficulty of performing reproducible and reliable measurements in systems with hysteresis. Therefore, the impact of measurement parameters on the measured hysteresis is investigated. Furthermore, an initialization routine is introduced which enables reproducible measurements on OTFTs.

Although the operation of field–effect transistors necessarily depends on a capacitive coupling between the gate electrode and the active material, investigations on capacitance-voltage (C–V) characteristics of OTFTs are rare in the literature. Therefore, Chapter 4 focuses on the quasi-static capacitance-voltage (QSCV) characteristics of organic metal-oxide-semiconductor (MOS) structures. Following the basics of C–V characteristics of organic MOS capacitors, a brief review on limited number of previous studies in the literature is given. After the experimental details on fabrication and electrical measurements of MOS capacitor probes, measured QSCV characteristics are presented. In addition to hysteresis, an unfamiliar plateau is present in the characteristics which are further investigated in this chapter. A behavioral model is also introduced which can be utilized to simulate the QSCV characteristics of various organic capacitor structures.

Chapter 5 concludes the thesis and provides an outlook for possible future work.

Chapter 2

Theoretical Background

The primary aim of this chapter is to introduce the chemical physics of organic materials in a simple but comprehensive manner such that the charge transport phenomenon in organic molecules can be understood without any existing organic chemistry expertise. For this purpose, we start with the basics of atomic and chemical bonding theories and progress through more complex concepts such as hybridization and conjugation. Next, energy diagrams of organic molecules are reviewed and the formation of trap and charge transport states is described. Molecular orbital theory is utilized to explain the semiconducting properties of organic molecules and their thin-films. Finally, these understandings are employed to introduce various charge transport mechanisms in organic semiconductors.

The second part of the chapter deals with the organic thin-film transistors (OTFTs). Following a brief explanation of the operation principles of a field-effect transistor (FET), different operation regimes of an OTFT are introduced and principle device geometries are presented. A detailed literature survey on functional material types with an emphasis on the processibility, stability, and performance follows, which summarizes the state-of-the-art organic materials having been reported in recent research articles. Next section introduces OTFT fabrication techniques with focus on substrate preparation, thin-film deposition, and patterning issues. Finally, the electrical characterization of OTFTs and the measurements performed to study current-voltage (I–V) and capacitance-voltage (C–V) characteristics are described.

2.1 Organic Semiconductors

Plastics are well-known insulators. Yet, the Nobel Prize awarded study from Shirakawa, MacDiarmid and Heeger showed that semiconducting and conducting plastics can be synthesized by controlling the conductivity through doping.[1] Since then a vast number of semiconducting plastics have been reported.[4,11] Due to their carbon-based backbone these semiconductors are called "organic" referring to the organic chemistry, which deals with carbon-based compounds, hydrocarbons and their derivatives.

Organic semiconductors can be divided into two classes depending on the length of the molecule. Polymers are macromolecules with long chains which consist of repeating units called monomers. Oligomers, on the other hand, consist of only a few–usually up to 8 to 10–monomers, which are also known as small molecules. Independent of the molecule size, the conductivity of semiconducting plastics is due to the favorable chemical properties of the carbon atom in the covalently bonded backbone. Carbon has a moderate electronegativity which allows it to form strong covalent bonds with other carbon atoms. As a group IV atom in the periodic table, it can form up to four bonds which not only enhance the stability of the molecule but also increase its chemical versatility. Last but not least, carbon hybridizes into a number of geometries to form single, double and triple bonds as well as a range of resonance bonding configurations.[12] In the following, we introduce some basic concepts to explain the chemical physics of carbon based organic semiconductors.

2.1.1 Covalent Bonding and Hybridization

According to the electron cloud model an atom consists of a nucleus surrounded by orbiting electrons. These electrons exist in so called atomic orbitals, which describe regions in space where the electrons occupying an orbital are likely to be found.[13] According to Pauli Exclusion Principle each atomic orbital can hold a maximum of two electrons and can be described as empty (no electrons), half-filled (one electron) or filled (two electrons). When two half-filled valence atomic orbitals of two different atoms overlap a covalent bond is formed. The electrons in the overlapping orbitals get paired and confined between the nuclei of the two bonding atoms. Depending on the geometry of the overlapping, two types of covalent bonding can be defined, which are illustrated in Fig. 2.1 using an oxygen molecule as an example. A neutral oxygen atom has six valence

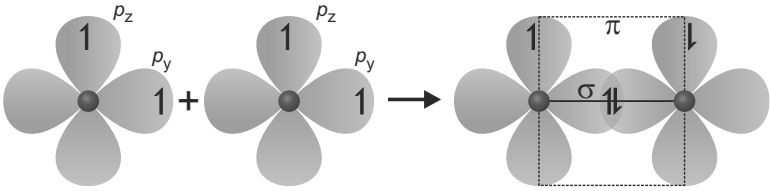

Figure 2.1. The formation of a double covalent bond between two oxygen atoms. The overlapping of half-filled p_y atomic orbitals along the internuclear axis forms a sigma (σ) bond while the sidewise interaction of p_z atomic orbitals forms a pi (π) bond. Half arrows show the spins of electrons residing in an orbital.

electrons which are distributed among s and p atomic orbitals such that each atom has two filled (s, p_x) and two half-filled atomic orbitals (p_y, p_z). For the sake of clarity, only the half-filled atomic orbitals, which are capable of forming a covalent bond, are illustrated in Fig. 2.1. The covalent bond formed due to the overlapping of p_y atomic orbitals along the internuclear axis is called a sigma (σ) bond. It is a strong bond since bonding electrons are strongly attracted by the nuclei of both bonding atoms. The covalent bond formed by sidewise overlapping of p_z atomic orbitals is called a pi (π) bond. In this bond type, the overlapping regions of bonding orbitals lie above and below the internuclear axis. It is relatively a weaker bond since the electron of each bonding atom does not strongly interact with the nucleus of other bonding atom.[13,14]

As a group IV atom the ground state electron configuration of carbon is $1s^2 2s^2 2p_x^1 2p_y^1$. It has four valence electrons and needs four more to reach a noble gas electron configuration. However, only two of the four valence electrons are unpaired which allows it to form only two bonds. In order to form four bonds, there must be four unpaired electrons. This arises when one of the $2s$ electrons is excited to the empty $2p_z$ orbital resulting in the following excited state electron configuration $1s^2 2s^1 2p_x^1 2p_y^1 2p_z^1$ with four half-filled valence atomic orbitals. During this rearrangement, s and p atomic orbitals with different characteristics interact to give a set of new degenerate (equivalent in energy) orbitals. This intermixing of two or more different atomic orbitals of an atom is called hybridization and the new orbitals are called hybrid orbitals.[15] During hybridization the total number of orbitals and the total energy of the system are preserved. Therefore, in case of carbon, the energy of hybrid orbitals is somewhere between that of s and p orbitals depending on the number of p orbitals which participate in hybridization (Fig. 2.2).

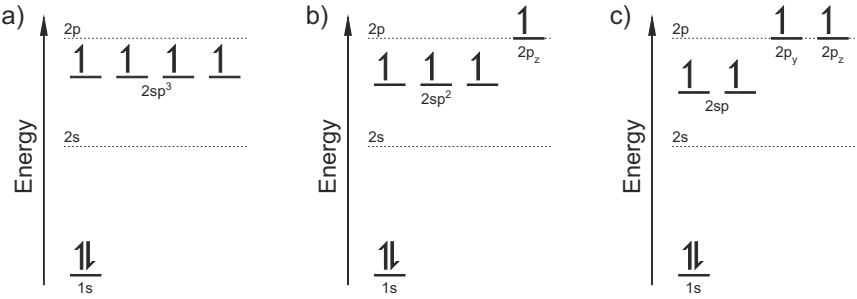

Figure 2.2. Energy diagram of (a) sp^3, (b) sp^2, (c) sp hybridized orbitals of a C atom.

Carbon can go through sp, sp^2 and sp^3 hybridizations.[13] In the example of methane (CH_4), carbon forms single covalent bonds through its four sp^3 hybrid orbitals. Each hybrid orbital of carbon overlaps with the s orbital of a hydrogen (H) atom forming a total of four σ-bonds which give the molecule a tetrahedral geometry (Fig. 2.3). In case of sp^2 hybridization, only the $2p_x$ and $2p_y$ atomic orbitals mixes with the $2s$ orbital forming three trigonal planar aligned sp^2 hybrid orbitals. The remaining unhybridized p_z orbital aligns perpendicular to the trigonal plane. For example, in ethylene (C_2H_4) molecule both carbon atoms are sp^2 hybridized. Each of two of the three sp^2 hybrid orbitals of each carbon atom forms a covalent bond to a hydrogen atom while the third hybrid orbitals overlap with each other to form a σ-bond between the nuclei of carbon atoms. By sharing the electrons of the half-filled p_z orbitals a weaker π-bond is also formed, which explains the double bond between carbon atoms in ethylene. Carbon can also go through sp hybridization where only the $2p_x$ orbital mixes with $2s$ orbital to form two sp hybrid orbitals of planar geometry. The remaining unhybridized p_y and p_z orbitals align perpendicular to each other and to hybrid orbitals. In this manner, two sp hybridized carbon atoms form a triple covalent bond, with one σ-bond of overlapping hybrid orbitals and two π-bonds of unhybridized p orbitals, as in acetylene (C_2H_2).[13]

2.1.2 Conjugation and Basics of Charge Transport in Organic Molecules

Most organic semiconductors have sp^2 hybridized carbons in their structure. This is due to the aptitude of sp^2 hybridized carbons to form alternating single and double bonds along the molecular backbone. Since π electrons of double

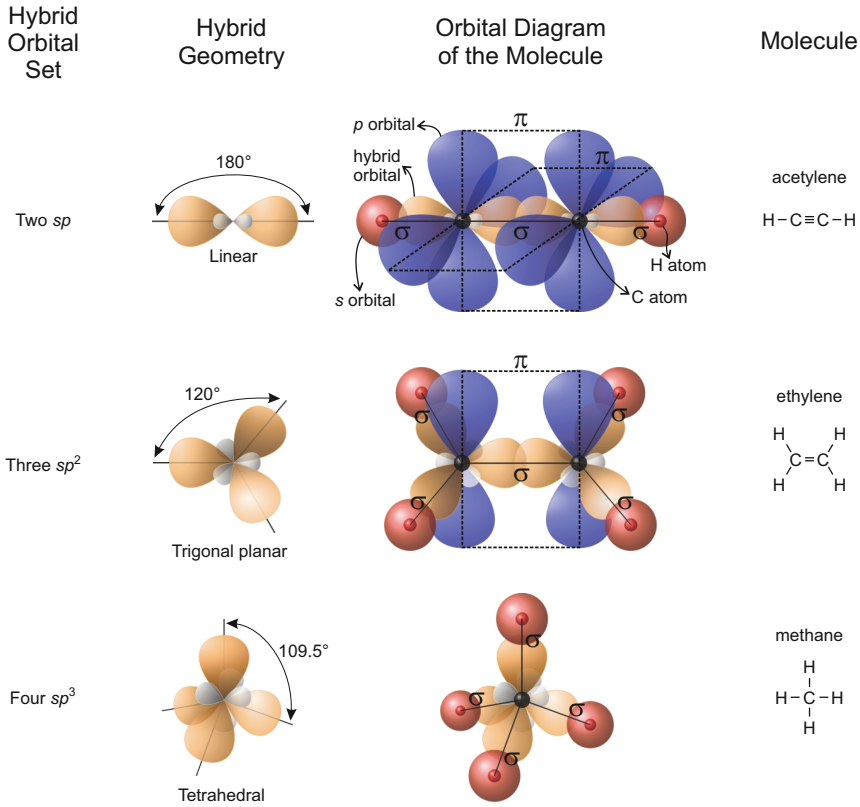

Figure 2.3. Various hybridizations of carbon atom

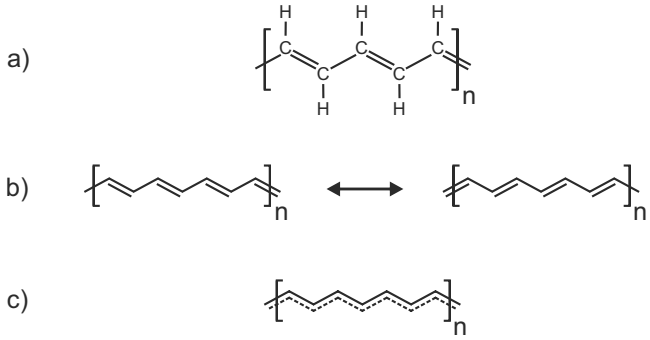

Figure 2.4. (a) Structural diagram of polyacetylene (b) Degenerate resonance states of polyacetylene (c) Delocalization of π electrons along the backbone.

bonds are weakly interacting with each other, π-bonds can switch between neighboring atoms which leads to resonance forms of a molecule. As in the case of polyacetylene (Fig. 2.4a), resonance forms can be degenerate where none of the resonance forms is energetically more favorable (Fig. 2.4b). In such systems, π electrons do not belong to a bond or an atom, but they are delocalized along the carbon backbone forming a one dimensional (1-D) electronic system (Fig. 2.4c). Such kind of delocalization of π electrons in systems with alternating single and double bonds is called conjugation and it is of prior importance for the 1-D charge transport in organic materials.

Yet, in order to understand why conjugated materials are semiconductors we should once again refer to the orbital theory. When atoms come together to form molecules through chemical bonding, their overlapping atomic or hybrid orbitals combine to form molecular orbitals. For each orbital of each bonding atom a new molecular orbital will be formed. Similar to atomic orbitals, molecular orbitals describe regions in space where the electrons of a molecule are likely to be found. Due to the wave-like behavior of electrons, atomic orbitals can overlap either constructively (in-phase) or destructively (out-of-phase). A constructive interference between atomic orbitals leads to a "bonding" molecular orbital as the probability to find an electron between the nuclei of bonding atoms increases. The fact that the electrons in the internuclear space will be attracted from positively charged nuclei of both bonding atoms lowers the energy of the molecule resulting in a stable bond. In case of a destructive interference, the probability to find an electron between the nuclei decreases, therefore, the probability to find it

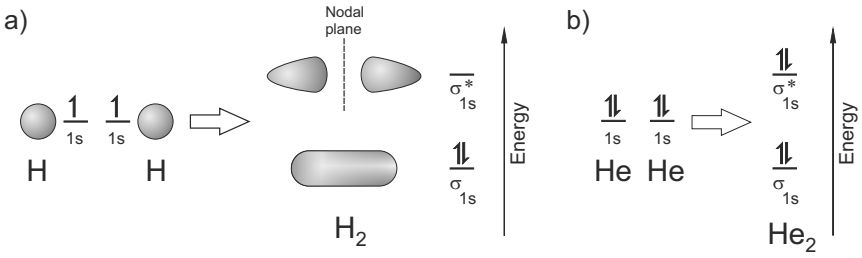

Figure 2.5. Energy diagrams for selected diatomic molecules. (a) Atomic orbitals for hydrogen (H) and molecular orbitals–both bonding (σ) and anti-bonding (σ^*)–for dihydrogen (H_2). (b) Energy diagram for helium (He) and dihelium (He_2).

outside of the internuclear space increases. The resulting arrangement does not favor bonding since with the missing electron in between, nuclei repel each other and atoms are forced apart. Thus, the net energy of the molecule increases. Such out-of-phase interference of atomic orbitals results in an "anti-bonding" molecular orbital.

When two atomic orbitals overlap, both bonding and anti-bonding molecular orbitals are always formed. Yet, how the electrons will be distributed to these orbitals depends on the electron configurations of bonding atoms. For example, in case of H_2, both hydrogen atoms have half-filled s orbitals, therefore, both of the two bonding electrons occupy the lower energy bonding sigma (σ) molecular orbital, while the higher energy anti-bonding sigma (σ^*) molecular orbital remains empty (Fig. 2.5a). However, if there are more electrons available, as in the example of He_2, electrons also occupy the anti-bonding sigma (σ^*) molecular orbital (Fig. 2.5b). Since the energy of anti-bonding sigma (σ^*) electrons are higher than the energy of s orbital electrons of He atom, this configuration is not energetically favorable and He_2 molecule does not exist in a stable form.

Now we can have a look at the electron configuration of ethylene (C_2H_4) to understand the semiconducting properties of polyacetylene. In ethylene each C atom builds a σ-bond with two H atoms and a double bond, which consists of a σ and a π-bond, with the other C atom (see Fig. 2.3). Thus, a total number of six bonding molecular orbitals (MOs) with three different energy levels, depending on the covalent bonding type and the electronegativities of the bonding atoms, are formed, namely,

- 1 bonding sigma (σ_{C-C}) MO from sp^2 hybrid orbitals of both C atoms,

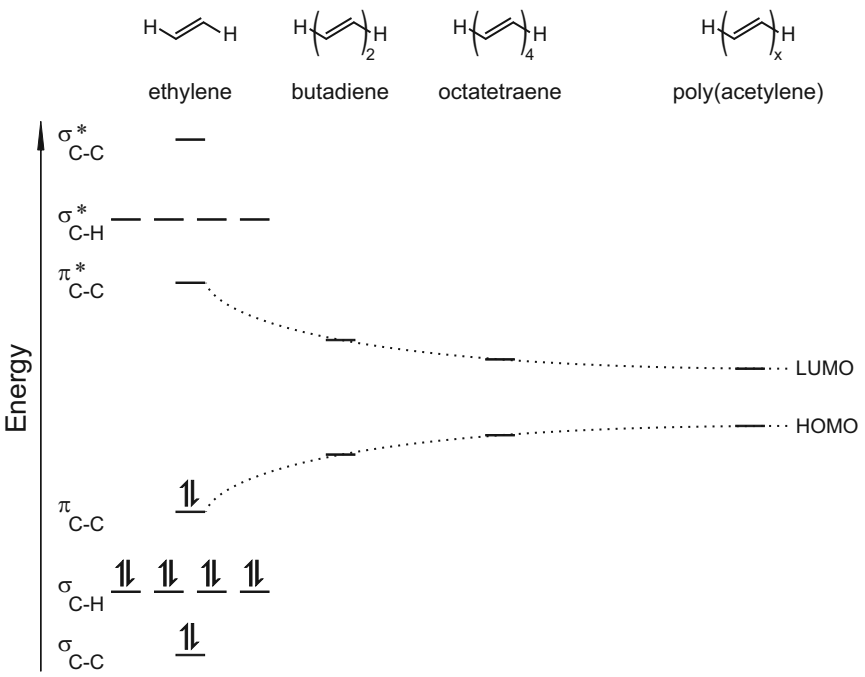

Figure 2.6. Energy diagram for the molecular orbitals of ethylene and the change in the band gap for molecules with higher numbers of ethylene monomers.

- 4 bonding sigma (σ_{C-H}) MOs, each from an sp^2 hybrid orbital of a C atom and s orbital of a H atom,
- 1 bonding pi (π_{C-C}) MO from unhybridized p_z orbitals of both C atoms (Fig. 2.6).

For each bonding MO a corresponding anti-bonding MO forms, as well. Hence, a total of 12 electrons (4 from each of two C atoms and 1 from each of four H atoms) fill the MOs starting from the lowest energy level - two at a time in accordance with the Pauli Exclusion Principle. In the resulting electronic configuration the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) are of primary importance since the energy levels of these MOs and the energy gap in between determine the electrical and optical properties of the conjugated materials analogous to the band gap between the valence and the conduction band in inorganic semiconductors.

As it can be seen in Fig. 2.6, the energy gap of ethylene is determined by the energy levels of the bonding and the anti-bonding π-MOs, which corresponds to the HOMO and LUMO levels, respectively. This is the reason why the delocalized π-electron system governs the electrical properties of ethylene and all other conjugated molecules.

The energy gap of a single ethylene molecule is 11.87 eV, which is far above the range to expect it to present semiconducting properties. However, it has been shown that the band gap decreases for longer molecules which consist of higher numbers of ethylene monomers, e.g. $\sim$ 9.7 eV for butadiene (C_4H_6) and $\sim$ 8 eV for octatetraene (C_8H_{10}).[16] If one follows this trend, the decrease in the energy gap with the increasing conjugation length along the carbon backbone, poly(acetylene) would be expected to show one dimensional (1-D) metallic conductor properties without any band gap. However, 1-D metals are not stable. Lattice vibrations and dimerization disturb the 1-D π-electron system by changing the spacing between adjacent atoms which opens a band gap. Therefore, poly(acetylene) is a 1-D semiconductor with a moderate band gap of $\sim$ 1.4 eV.[17]

Except for poly(acetylene), most conjugated polymers contain rings of carbon atoms. In some configurations, a different atom, such as sulphur or nitrogen, substitutes one of the carbon atoms. Side chains, which hardly affect the electronic properties, can be covalently connected to the polymer backbone in order to control physical properties such as crystallinity and solubility. Some of the repeating functional units in conjugated organic materials, which are common for organic electronics research, are given in Fig. 2.7. In order to explain the electronic properties of similar material, we will investigate the benzene molecule.

Benzene consists of six sp^2 hybridized carbon atoms in a ring arrangement

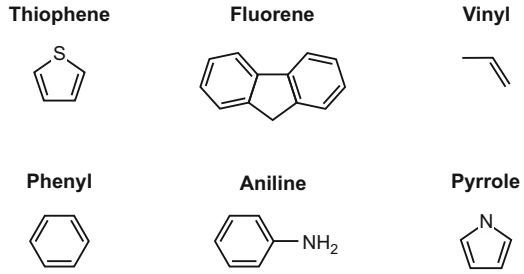

Figure 2.7. Some of the common repeating functional units in conjugated organic materials. Adapted from Ref. [12].

of alternating single and double bonds, where each C atom also forms a σ-bond with an H atom. Similar to poly(acetylene), it is conjugated along the carbon backbone and it has two degenerate resonance forms where none of these is energetically more favorable (Fig. 2.8). Due to the delocalized π-electron cloud, 1-D charge transport is possible along the ring structure.

In order to investigate the semiconducting properties of benzene, we once again refer to the molecular orbital (MO) diagrams. For the sake of simplicity, in schematic diagrams only the delocalized π-electrons are presented since, as mentioned before, they dominate the electrical properties of conjugated molecules. The overlapping p_z atomic orbitals of C atoms in benzene form six MOs - three lower energy bonding MOs and three higher energy anti-bonding MOs (Fig. 2.9). Due to different possible overlap configurations of six atomic orbitals - remember the in-phase and out-of-phase interaction of atomic orbitals mentioned previously in this section - bonding MOs quantize in energy, forming a bonding MO with the lowest energy, where the in-phase overlap is greatest, and two degenerate bonding MOs with higher energy. Analogously, anti-bonding MOs also quantize in energy, forming an anti-bonding MO with the highest energy and two degenerate anti-bonding MOs with less energy. Starting from the lowest energy MOs, six π-electrons of the delocalized system occupy MOs in pairs, resulting in a fully occupied set of bonding MOs and an empty set of anti-bonding MOs. Thus, higher energy bonding MOs and lower energy anti-bonding MOs set the HOMO and LUMO level of benzene molecule, respectively. The band gap of a single benzene molecule is calculated to be relatively large. i.e. $\sim 10.5\,\text{eV}$. However, similar to the case in conjugated polymers, the band gap decreases with increasing size of the conjugated system, which is observed in single molecules with higher numbers of benzene rings (Fig. 2.9), e.g. $\sim 8.3\,\text{eV}$ for naphthalene, $\sim 6.9\,\text{eV}$ for anthracene, $\sim 6.1\,\text{eV}$ for tetracene, $4.5\,\text{eV}$ (theoretical) to $5.2\,\text{eV}$ (experimental) for pentacene.[18,19] Yet, even in longer molecules with larger conjugated systems, the HOMO-LUMO gap is quite wide ($\sim 4\,\text{eV}$) to have semiconducting charac-

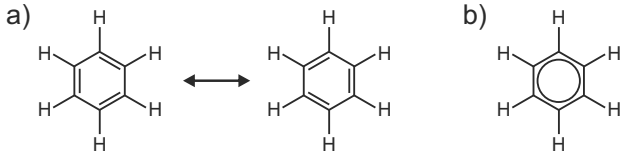

Figure 2.8. (a) Resonance states of benzene (b) Delocalization of π-electrons along the backbone.

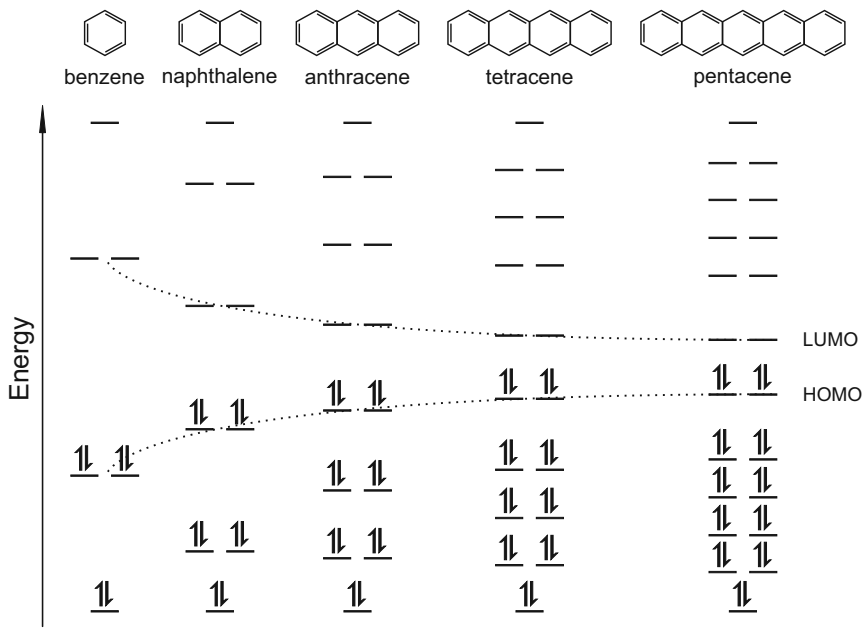

Figure 2.9. Energy diagram for π molecular orbitals of a single benzene molecule and the change in the band gap for molecules with higher numbers of benzene rings.

teristics at room temperatures. Fortunately, the electronic picture improves when we consider the thin films where many conjugated molecules are densely packed. Intermolecular electron delocalization across the closely packed conjugated molecules narrows the HOMO-LUMO gap while the interactions between MOs of adjacent molecules result in splitting of HOMO and LUMO, which leads to the formation of semi-continuous narrow energy bands consisting of many discrete energy levels. Thus, for example, in polycrystalline pentacene thin-films, HOMO-LUMO gap decreases to $\sim 2.2\,\mathrm{eV}$.[19] Furthermore, HOMO and LUMO levels split to form narrow bands of $\sim 0.6\,\mathrm{eV}$, which are analogous to the valence band and conduction band in inorganic semiconductors.[20]

2.1.3 Charge Carriers and Trap States in Conjugated Materials

So far we have discussed the formation of electronic bands in conjugated materials which enables the charge transport. However, it should still be explained how

charge carriers are formed in these materials. In inorganic semiconductors this is commonly achieved through doping, which is the substitution of a lattice atom with an extrinsic atom, which is either in excess of an electron (n-type doping) or missing an electron (p-type doping) compared to the lattice atom. Therefore, the charge carriers in doped inorganic semiconductors are either the electrons in the conduction band or the missing electrons (holes) in the valence band. The same analogy is also used for conjugated materials, though misleading, since the "doping" is rather due to redox reactions and not because of lattice substitutions. In organic semiconductors an oxidizing agent introduces a cation to the carbon backbone by removing a weakly bound π-electron which corresponds to p-type doping in solid-state physics terminology. Analogously, a reducing agent which introduces an anion by adding a π-electron equals n-type doping.[21]

However, due to the coulombic interactions, the removed (or introduced) charge induces a local lattice distortion around itself. This quasi-particle, which consists of a charge associated with a lattice distortion, is called a polaron. The distorted lattice leads to modification of the π-electron system forming localized electronic states in the band gap (Fig. 2.10). Two polarons can confine to the same lattice distortion to reduce their overall energy. If these polarons carry opposite charges, the coulombic bound state of them is called a polaron exciton. Even if similar charges repel by the coulombic interaction, sharing the same lattice distortion can be energetically favorable for polarons with the same charge such that a net attractive force exists between these. The resulting bound state of two polarons of the same charge is called a bipolaron. Since the lattice distortion around two charges is stronger than around one charge, bipolaron electronic states are further away from HOMO-LUMO edges in the band gap (Fig. 2.10). In case of a degenerate polymer, such as trans-(poly)acetylene, bipolarons can separate without having any energetic penalty since both resonance forms between and on the other sides of the two charges are energetically equivalent. This leads to the formation of a soliton with a localized electronic level at midgap (Fig. 2.10).[22–24]

In addition to the above mentioned electronic states of charge carriers, there exist strongly localized states in the band gap of organic semiconductors, which are known as trap states, where mobile charge carriers can get captured and, therefore, localized for a definite time.[22,25] Trapped carriers cannot take part in charge conduction, thus, trap states strongly affect the charge transport in organic materials since the charge transport through single energy levels is very

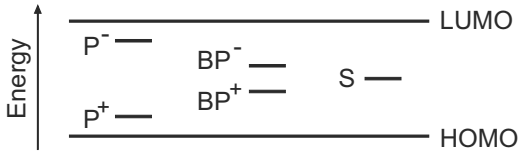

Figure 2.10. Energy levels of polaron (P), bipolaron (BP), soliton (S) in the band gap. "−" and "+" symbols show the possible energy levels for electrons and holes, respectively.

vulnerable to the interruptions in the electronic systems. Depending on the capture/release rates and the average trapping time, trapped carriers lead to delayed electrical responses and hysteresis, which is explained in detail in Chapter 3.

There are several sources for trap states. For example, impurities, which cannot be avoided during organic polymer synthesis, can easily introduce trap states by disturbing the π-electron conjugation along the backbone. On the other hand, most organic semiconductors form polycrystalline or even amorphous films in condensed form. Therefore, even in absence of impurities, structural imperfections lead to discrete trapping levels in the band gap. Interfaces, where the chemical structure abruptly terminates leaving boundary atoms with unsaturated dangling bonds, are also known to induce trap states. Even the strong electron-phonon coupling in a polaron can be considered as a self trapping state since the lattice deformation, which travels with the charge carrier, reduces its movability.[26]

Trap states can differentiate according to the position of their energy levels in the band gap.[27] A localized state below the LUMO energy level, which is able to capture an electron, is called an electron trap, whereas a localized state above the HOMO energy level, which is able to capture a hole, is called a hole trap. For each kind of traps, a further distinction can be made between shallow and deep traps depending on the energetic separation of a trap state from the next available transport state, i.e. the HOMO or the LUMO edge (Fig. 2.11).[7] Due to amorphous structure of organic films there are also some localized states above the LUMO and below the HOMO energy levels. These, so called antitraps, cannot trap charges since it would be energetically unfavorable; however, they result in scattering centers which also affect the charge transport in organic materials.[28]

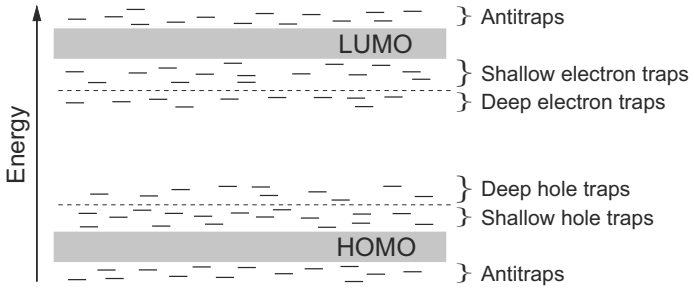

Figure 2.11. Energetic distribution of trap and antitrap states in organic materials.

2.1.4 Charge Transport Mechanisms in Organic Semiconductors

In crystalline solids, energy bands occur when a large number of interacting atoms are brought together. These energy bands are wide due to the favorable overlap of atomic orbitals owing to the almost perfect repeatability in the crystal lattice arrangement. In organic materials, bands are narrow and the discrete energy levels within the bands are more prominent. Therefore, in addition to the coherent band-like transport along a molecule, incoherent hopping transport through localized discrete energy states is probable in organic semiconductors. In the following we will introduce the basics concepts of charge transport in organic materials.[29–33]

2.1.4.1 Band Transport

Band transport depends on formation of allowed and forbidden energy bands through the overlap of spatially and energetically closely packed energy levels of a material in solid state. Starting from the lowest energy levels, these bands are filled with electrons up to a temperature specific energy level. At absolute zero temperature (0 K), the highest occupied band (valence band) is completely filled while the lowest unoccupied band (conduction band) is completely empty. At nonzero temperatures, electrons gain energy with increasing temperature such that an electron at the top of the HOMO level can be thermally excited to a state at the bottom of the LUMO leaving a hole behind (Fig. 2.12a). In case of an applied electric field, the excited electron and the hole are free to move along the delocalized states of the LUMO and the HOMO, respectively (Fig.

2.12c). In delocalized bands, charge transport is limited by scattering of charge carriers by phonons (lattice vibrations). Therefore, above a material specific critical temperature, charge carrier mobility in organic materials decreases with increasing temperature due to increasing phonon interactions.

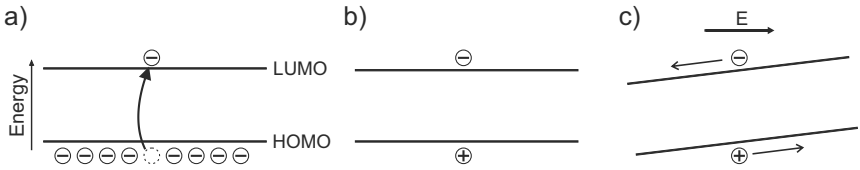

Figure 2.12. Schematic representation of band transport in organic materials. (a) An electron is thermally excited to the LUMO. (b) The missing electron in the HOMO can be represented with a hole. (c) If an electric field is applied, free charge carriers can move along the delocalized bands.

2.1.4.2 Tunneling

The conjugated π-electron system is the basis of charge transport in organic semiconductors. In organic molecules, strong covalent bonds along the carbon backbone favor the intramolecular charge transport. Yet, in solid phase, organic molecules are held together by the weak van-der-Waals forces. The resulting poor overlap between the electronic systems of adjacent molecules not only hinders the formation of broad charge transport bands but also leads to the localization of charge carriers on individual molecules. Thus, narrow, band-like energy levels consisting of localized states exist in organic solids.[26] In absence of continuous energy bands, charge transport between spatially and energetically separated states takes place by tunneling or hopping (Fig. 2.13). In case of tunneling, an excited charge carrier can penetrate through a potential barrier to a non-occupied state of a neighboring molecule. It is a quantum mechanical phenomenon based on the wave-particle duality of matter. The tunnel probability strongly depends on the width of the energy barrier and the applied electric field but is essentially independent of the temperature.[34]

2.1.4.3 Hopping

Another explanation for the charge transport between localized states is hopping, where charge carriers move to the next available state by jumping over an

energy barrier (Fig. 2.13). Since the energy difference between two states can be overcome by absorption or emission of a lattice vibration (phonon), hopping is a phonon-assisted mechanism. Lattice vibrations increase with increasing temperature. Therefore, in case of hopping, which can be seen as thermally assisted tunneling, the charge carrier mobility increases with increasing temperature. Yet, especially at low temperatures, a charge transfer over long distances may become energetically more favorable than a transfer to higher nearby energy states. This leads to the variable-range hopping model, which explains the charge transport between localized states in disordered organic semiconductors.

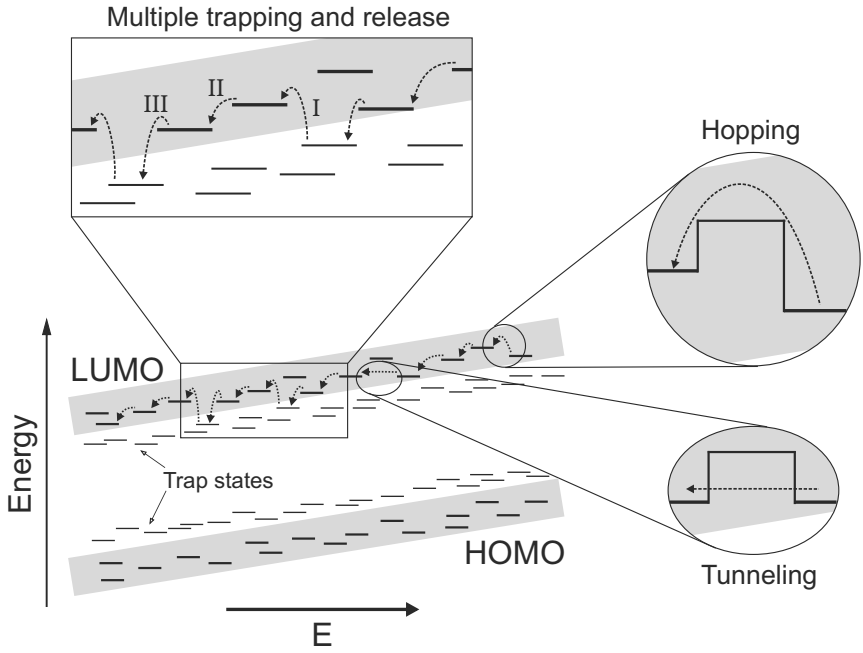

Figure 2.13. Schematic representation of various charge transport models in organic materials. By tunneling a charge carrier penetrates through a potential barrier while by hopping it jumps over the barrier. By multiple trap and release (MTR) model, a charge carrier on a trap state is first thermally activated to a delocalized transport band (I), where it can drift with the applied electric field (II) before it gets captured in another trap state (III).

2.1.4.4 Multiple Trapping and Thermal Release

The last charge transport model we want to introduce for organic semiconductors is the multiple trapping and thermal release (MTR) model which, unlike previous models, takes the effect of traps into consideration.[7] It is similar to tunneling and hopping transport in the sense that charge carriers are transferred between localized energy states. However, in this case, a charge carrier on a localized state does not move directly to the next available state but it is first thermally activated to a delocalized transport band, where it drifts with the applied electric field, before it gets captured in another trap state (Fig. 2.13). As the charge carriers are thermally activated to transport levels, the charge carrier mobility is expected to increase with increasing temperature.

It should be noted at this point that none of the charge transport models introduced above can solely explain the experimental observations on organic semiconductors for different temperature ranges and trap concentrations. Therefore, we conclude that the nature of charge transport in conjugated materials is still controversial and it strongly depends on the intrinsic and extrinsic parameters such as charge carrier concentration, unintentional doping, spatial and energetic distribution and concentration of traps, temperature, and morphology.

2.2 Organic Thin-Film Transistors

An organic thin-film transistor (OTFT) is a field-effect transistor where at least the active material is a thin-film of an organic material. It is a common practice in the literature to quote an inorganic transistor structure as an organic transistor if the active layer is an organic semiconductor. Yet, some authors prefer to call such a device “hybrid” transistor, whereas the term “all organic” is used for a transistor which is solely made of organic materials.

This section aims to provide some background information on thin-film transistors. The first subsection introduces the operation principles and the device geometry of OTFTs. A detailed literature review on materials, which are used to fabricate OTFTs, follows. The fundamentals of OTFT fabrication are summarized in the next subsection. The measurement routines, which are used to study the organic device characteristics in this thesis, are introduced in the last part of the section.

2.2.1 Basics of Operation

Analogous to a metal-insulator-semiconductor (MIS) field-effect transistor (FET), the basic idea of an organic FET is to control the conductivity of a semiconducting material which is capacitively coupled to a conducting electrode, the gate electrode, via a thin insulating layer, the gate insulator. When a voltage is applied to the gate electrode, a sheet of mobile charge carriers accumulates at the semiconductor-dielectric interface, forming a conductive channel between two ohmic contacts, the source and drain electrodes. Once the channel is formed, a current flows between the source and drain electrodes if a bias is applied between these. Since the conductivity of the channel, which is a function of the charge carrier density in the semiconductor, is capacitively coupled to the voltage at the gate electrode, the current flow between the source and drain electrodes can be modulated by the gate voltage.

Organic FETs are fabricated by depositing thin films of functional layers on different substrates. This is why they are also called organic thin-film transistors (OTFTs). OTFTs can be fabricated in different device configurations (Fig. 2.14). In a coplanar device, organic semiconductor is applied on pre-patterned electrodes, so that the source-drain contacts are on the same plane with the conducting channel. However, in staggered device configurations, the channel forms on the opposite side of the semiconducting film where the source-drain contacts are fabricated. The latter device configuration exhibits better device performance, mainly due to a lower contact resistance through larger contact area between contacts and the channel. Yet, in this geometry the organic semiconductor is more vulnerable to contaminations because of the fabrication steps which take place after the deposition of the semiconducting film. To prevent contaminations inverted (bottom-gate) coplanar device configuration is preferred, where the semiconductor is deposited as the final step.

In OTFTs, the source and drain electrodes are usually implemented by directly contacting the organic semiconductor with a metal. Depending on the energetic position of the HOMO-LUMO levels of the organic semiconductor and the work function of the contact metal, the injection and transfer of one charge carrier type, i.e. electron or hole, within the channel is favored, which determines whether the n-channel or p-channel operation dominates. Both kinds of device operation have been reported for OTFTs in the literature, however, p-channel operation outweighs since the atmospheric oxygen constrains n-channel operation by either unintentional doping of the organic semiconductor or oxidation of

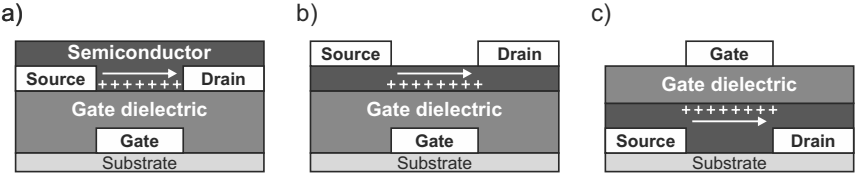

Figure 2.14. Schematic cross-sections of the three principle OTFT geometries. The accumulated channel is schematically shown with "+" signs while the arrow shows the direction of current flow. (a) Inverted (bottom-gate) coplanar geometry, (b) inverted staggered geometry, (c) top-gate staggered geometry. Adapted from Ref. [4].

the low work function contact metal.[4,35] This effect is further explained in the next subsection.

Although the formation of the conducting channel and the physics of charge transport along the channel are different, the current-voltage characteristics of OTFTs can be, to a good extent, described with the same formalism which was derived for MISFETs. For a p-channel transistor, the drain-source current (I_{DS}) reads

$$I_{\mathrm{DS}} = \begin{cases} -\mu \dfrac{W}{L} C_{\mathrm{i}}' \left[V_{\mathrm{GS}} - V_{\mathrm{th}} - \dfrac{V_{\mathrm{DS}}}{2} \right] V_{\mathrm{DS}} & \text{for} \begin{pmatrix} V_{\mathrm{GS}} < V_{\mathrm{th}} \\ V_{\mathrm{DS}} \geq V_{\mathrm{GS}} - V_{\mathrm{th}} \end{pmatrix} \\ -\mu \dfrac{W}{2L} C_{\mathrm{i}}' \left[V_{\mathrm{GS}} - V_{\mathrm{th}} \right]^2 & \text{for} \begin{pmatrix} V_{\mathrm{GS}} < V_{\mathrm{th}} \\ V_{\mathrm{DS}} \leq V_{\mathrm{GS}} - V_{\mathrm{th}} \end{pmatrix} \end{cases} \tag{2.1}$$

where V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, C_{i}' is the gate dielectric capacitance per unit area, μ is the charge carrier mobility, W is the channel width, and L is the channel length of the transistor. V_{th} is the threshold voltage, which is the gate bias required to induce a strong inversion according to the inorganic semiconductor analogy. Since OTFTs operate in accumulation but not in inversion mode, the threshold voltage is not defined for OTFTs, however, V_{th} can be used as a parameter which indicates the voltage at which a conducting channel of accumulated charge carriers forms.

According to (2.1), I_{DS} has two different regimes, i.e. linear and saturation regimes, which can be best observed in the output (I_{DS} vs. V_{DS}) characteristics (Fig. 2.15). In the linear regime, i.e. $V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{th}}$, charge carriers are so distributed that a continuous channel exists between the source and drain contacts. In this regime I_{DS} depends on both V_{DS} and V_{GS}. However, for very small V_{DS} values, I_{DS} increases almost linearly with V_{DS}. For a constant V_{GS},

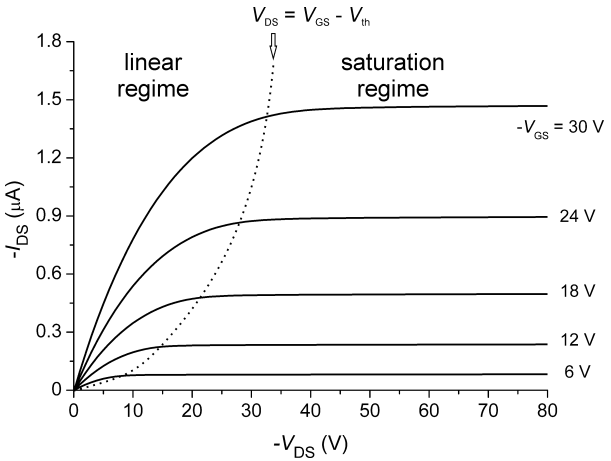

Figure 2.15. Measured output characteristics of a poly(3-hexylthiophene) (P3HT) based OTFT with $W/L = 500$. Different operation regimes according to (2.1) are shown.

increasing V_{DS} leads to a deviation from the linear behavior of I–V curves, as the increasing horizontal electric field between the drain and source electrodes enhances the charge carrier concentration gradient within the channel resulting in a lower concentration near the drain. When V_{DS} becomes equal to $V_{\mathrm{GS}} - V_{\mathrm{th}}$, the drain end of the channel is at the same electrical potential with the gate and the channel "pinches off" (disappears) at this point. Increasing V_{DS} further moves the pinch-off point towards the source and I_{DS} saturates, which means it becomes independent of V_{DS}. This operation regime, where I_{DS} does not increase with increasing V_{DS} is called the saturation regime.[34, 35]

2.2.2 Materials

Independent of the transistor geometry, three functional material types are necessary for an OTFT:

- a semiconducting material which forms the active layer,
- an insulator which serves as a gate dielectric by separating the gate electrode from the semiconducting active layer,
- highly conductive electrodes which either control the formation of a con-

ductive channel through an electric field, i.e. the gate electrode, or inject/remove charge carriers into/from the conductive channel, i.e. the source and drain electrodes.

Due to the diversity of organic molecules, numerous materials have been reported with regard to OTFT fabrication. In this subsection, we briefly summarize some of the intensively studied functional materials.

2.2.2.1 Semiconductors

Organic semiconductors can be grouped into a few classes according to a set of material properties such as, e.g. the molecular size (small molecules, oligomeres, polymers), the processibility (solubility) and the type of the predominant charge carrier in field-effect devices (electron, hole). In the following we introduce some organic semiconductors from each class to discuss their potential to be utilized in OTFTs.

Polymers are long molecules which consist of a repeating unit that can be functionalized with various side groups. For example, polythiophene (PT) is a semiconducting polymer, which results from polymerization of thiophene (C_4H_4S) molecules (Fig. 2.16). It is insoluble in most solvents in its unsubstituted form. However, the substitution of the hydrogen (H) at the 3-position of thiophene ring with an alkyl group (C_nH_{2n+1}) makes polythiophene soluble in most organic solvents. For example, hexyl (C_6H_{13}) substituted thiophene derivative poly(3-hexylthiophene) (P3HT) can be processed into thin films through various coating or printing techniques. Unless it is specifically synthesized to possess some high degree of regioregularity, P3HT forms amorphous films with short π-conjugation length, which leads to low charge carrier mobilities. Accordingly, the first organic transistor with regioregular head-to-tail P3HT had a charge carrier mobility of $0.01\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, which is two to three orders of magnitude higher than that of an OTFT with regiorandom P3HT.[36] Beside regioregularity, factors such as molecular weight, deposition conditions, surface energy of the substrate affect the size and arrangement of lamellar domains within the deposited film and hence the charge carrier mobility.[37,38] On the other hand, the low ionization potential of P3HT causes instable operation in ambient air since the atmospheric oxygen, which interacts with the polymer, degrades the π-electron conjugation along the polymer chain through photoinduced oxidation. Efforts to improve oxidation resistance and environmental stability have resulted in synthesis of further poly-

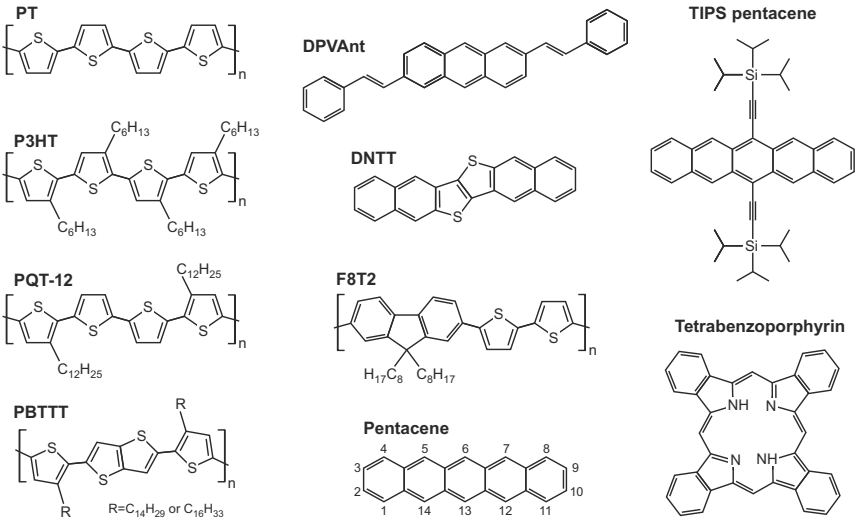

Figure 2.16. Structures of polymeric and small molecule organic semiconductors. Carbon positions are shown for pentacene. See text for details.

thiophene derivatives such as poly(3,3‴-didodecylquarterthiophene) (PQT-12) and poly[2,5-bis(3-alkylthiophen-2-yl)thieno-(3,2-*b*)thiophene] (PBTTT), with air stable carrier mobilities as large as $0.2\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $1.1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, respectively (Fig. 2.16).[39–41] With similar electrical properties, yet with improved solubility, polyflourenes constitute another class of conjugated polymeric semiconducting materials, whose HOMO-LUMO gap can be engineered through copolymerization with units like thiophenes as in the case of Poly[(9,9-dioctylfluorenyl-2,7-diyl)-co-bithiophene] (F8T2) with charge carrier mobilities up to $0.02\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (Fig. 2.16).[12,42,43]

Small molecules are also good candidates to be processed into thin films as the active layer in OTFTs. Compared to polymeric semiconductors, they are light and can usually be deposited to form polycrystalline films through thermal evaporation or organic vapor phase deposition (see Ref. [4] and references therein). Although insoluble in neutral form, many small molecule organic semiconductors can be functionalized to be soluble so that they can also be processed from solution.

Acenes, which are made up of linearly fused benzene rings, form a class of organic small molecules, which are know for their superior stacking properties.[12]

Among these molecules, pentacene, which is the organic semiconductor under study in this thesis, is by far one of the most extensively studied organic semiconductor in the literature (Fig. 2.16).[44] The good charge transport in pentacene has been explained with almost perfect overlap of frontier molecular orbitals within the molecules and herringbone packing of molecules in thin films grown on passivated low-energy surfaces.[7,45–47] However, pentacene is easily oxidized at the central benzene ring when exposed to ambient air.[48] Oxygen forms double bonds with carbon atoms at the 6 and 13 positions and degrades the π-electron system along the pentacene molecule which leads to lower charge carrier mobilities.[25,49]

In order to improve environmental stability, small-molecule semiconductors with larger ionization potentials than pentacene have been proposed. It has been shown that 2,6-di[2-(4-phenyl)vinyl]anthracene (DPVAnt) and dinaphtho-[2,3-*b*:2′,3′-f]thieno[3,2-*b*]thiophene (DNTT) have similar mobilities but much better stability in air (Fig. 2.16).[50–52] Another approach to improve air stability is to passivate the 6,13 positions of pentacene with bulky groups.[11,53] If the groups are properly selected, as in the case of tri-isopropyl-silylethynyl (TIPS) pentacene, the molecule is not only protected from oxidation but it also becomes soluble in common organic solvents (Fig. 2.16).[54–56]

Solubility is a key property for organic semiconductors since costly, time consuming evaporation steps can be avoided if a thin semiconducting film can be satisfactorily cast from solution. The idea to combine the simplicity of solution processing with the superior electrical properties of pentacene led to synthesis of soluble precursors which can be converted into pentacene through thermal annealing. The first pentacene precursor with tetrachlorocyclohexadiene is introduced by Brown *et al.* which was spin-coated from a dichloromethane solution.[57,58] The pentacene film was then formed by annealing at temperatures in the range of 140 °C to 200 °C for annealing times from 5 min to 2 h. Later with optimized annealing at 200 °C for 5 s, hole mobilities of 0.1 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and on/off ratios of 10^6 have been reported.[59] Since then other pentacene precursors with slightly higher mobilities have been demonstrated.[60–63] Yet, the mobility values remain behind that of evaporated pentacene films. The concept of soluble precursors has been further extended to other aromatic systems such as tetracene,[64] tetrabenzoporphyrin[65] (see Fig. 2.16), and polymers such as polyacetylene[66,67] and polythienylenevinylene (PTV).[6,57,68]

For all of the organic semiconductors we have presented so far, p-channel operation (hole transport) dominates in field-effect devices. This is because the

energy barrier between the HOMO energy level of the organic semiconductor and the work function of the source/drain contacts, which are usually fabricated from an air-stable metal such as gold, is usually much smaller than the barrier between the work function of the contacts and the LUMO level. In order to realize n-channel operation, the energy barrier which electrons need to overcome should be smaller than the barrier for holes. One approach to lower the energy barrier between the work function of the contacts and the LUMO while increasing the barrier between the work function of the contacts and the HOMO is to use low work function metals for contacts. For example, electron mobilities as large as $0.19\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $1.7\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $6\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ have been reported for pentacene,[69] α,ω-diperfluorohexylcarbonyl-quaterthiophene (DFHCO-4T),[70] pentacene-buffered fullerene C_{60}[71] for TFTs with calcium (Ca), gold (Au) and magnesium (Mg) electrodes, respectively (Fig. 2.17). However, these transistors can only be operated in vacuum since low work function metals and organic semiconductors with low electron affinities oxidize quickly in ambient atmosphere which profoundly degrades either the charge carrier injection from contacts into the organic semiconductor or the charge transport within the semiconductor. Therefore, another approach to match the work function of the contacts with the conduction band of the semiconductor is to introduce an ultrathin, interfacial electric dipole layer which results in a vacuum level shift at the metal/semiconductor interface.[72,73] Yet, such an attempt to match the work functions should be customized for every different metal-organic semiconductor pair which adds another step of complexity to OTFT fabrication. Consequently, efforts to develop n-channel OTFT has focused on synthesis of new organic semiconductors with higher LUMO levels, i.e. larger electron affinity.

Bao *et al.* synthesized hexadecafluorocopperphthalocyanine (F_{16}CuPc)[74] by substituting all 16 hydrogen atoms of copper phthalocyanine (CuPc) with fluorine (F) atoms which increased the electron affinity of the molecule to about 4.5 eV (Fig. 2.17).[75] This material not only shows very stable transistor operation in air without any encapsulation but also allows air-stable, high work function metals, such as gold, to be used for source/drain contacts. However, the reported electron mobilities of $0.08\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ is almost two orders of magnitude smaller than the best reported hole mobilities for OTFTs.[76] The poor mobility value has been explained with the disordered film growth at the dielectric interface where the active charge transport takes place during OTFT operation.[77]

The breakthrough towards air-stable n-channel operation was made with bis(2, 2, 3, 3, 4, 4, 4-heptafluorobutyl)-dicyano-perylene tetracarboxylic diimide (PTCDI–$(CN)_2$–$CH_2C_3F_7$) which had an electron mobility of $0.64\,cm^2\,V^{-1}\,s^{-1}$ in air (Fig. 2.17).[78,79] Later Schmidt *et al.* synthesized (PTCDI–$CH_2C_3F_7$) by removing the cyano (CN) groups from the bay positions of the conjugated core, which resulted in an electron mobility of $1.2\,cm^2\,V^{-1}\,s^{-1}$ with excellent air stability.[80] In addition to the above mentioned insoluble n-channel organic semiconductors, which can only be deposited through vacuum deposition, soluble alternatives have also been studied. A soluble fullerene derivate, phenyl–C_{61}–butyric acid methyl ester (PCBM), has been shown to reach an electron mobility of $0.21\,cm^2\,V^{-1}\,s^{-1}$ in OTFT configuration (Fig. 2.17).[81] Yet, the device degrades rapidly upon exposure to ambient air.[82] Furthermore, polymers have also been employed as electron transporting active layer. Excellent air stability has been reported for OTFTs made from poly{[N,N′-bis(2-octyldodecyl)-naphthalene-1, 4, 5, 8-bis(dicarboximide)-2, 6-diyl]-alt-5, 5′-(2, 2′-bithiophene)} (P(NDI2OD-T2)) with electron mobilities up to $0.85\,cm^2\,V^{-1}\,s^{-1}$.[83]

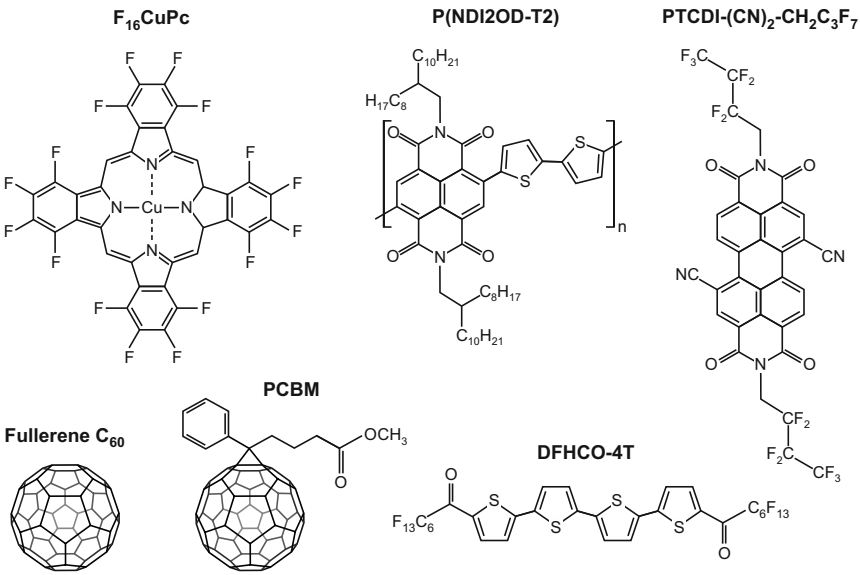

Figure 2.17. Structures of selected organic semiconductors which have been reported to support n-channel operation. See text for details.

A more detailed review on organic semiconducting materials can be found in recent review papers from Hagen Klauk[4] and Dong *et al.*,[11] or in an extensive chapter on design, synthesis and performance of organic semiconductors in the renowned textbook "Organic Field-Effect Transistors".[7]

2.2.2.2 Dielectrics

Properties of a good dielectric material can be summarized as high dielectric constant, high dielectric breakdown strength and the ability to form smooth, pinhole-free, thin films with low leakage currents. The thickness of the dielectric and its dielectric constant determine together the capacitively coupling between the gate electrode and the semiconductor, hence the amount of charge induced in the active layer. The dielectric strength sets the highest applicable gate bias before dielectric breakdown occurs. And, finally, the morphology of the dielectric affects the morphology of the thin semiconducting film which is deposited on top of it in bottom-gate device configurations. Therefore, the characteristics of the gate dielectric play an important role in the performance of OTFTs.

Due to its high resistivity ($\sim 10^{15}\,\Omega\,\mathrm{cm}$), very high dielectric breakdown strength ($> 10\,\mathrm{MV/cm}$) and superior thermodynamic stability, thermally grown silicon dioxide (SiO_2) used to be the prominent dielectric material for CMOS technology.[84] Since it can easily be grown on highly doped silicon, which serves as the gate electrode, SiO_2 has evolved as a reliable dielectric material for OTFT research despite its relatively low dielectric constant ($k = 3.9$). Other inorganic dielectrics with higher dielectric constants (high-k materials) such as barium zirconate titanate (BZT; $k = 17.3$),[85] barium strontium titanate (BST; $k = 16$),[85] tantalum pentoxide (Ta_2O_5; $k \sim 21 - 25$),[86,87] titanium dioxide (TiO_2; $k = 41$),[88] aluminum oxide (Al_2O_3; $k \sim 8 - 11$),[88,89] hafnium oxide (HfO_2; $k = 11$)[90] have been reported. Since most of these materials are brittle in bulk form, ultra-thin films ($\sim 100\,\mathrm{nm}$), which are suitable for flexible applications, have been prepared by electrochemical anodization or sputtering. Yet, solution-processibility is an important asset for OTFT applications. Therefore, gate dielectrics made of polymeric materials have been intensively studied.

The first report on polymeric insulators for OTFTs dates back to 1990 where Peng *et al.* demonstrated good I–V characteristics for devices with poly(vinyl alcohol) (PVA; $k = 7.8$)[91] and cyanoethylpullulan (CYEPL; $k \sim 15.4 - 18.5$)[91,92] gate dielectrics (Fig. 2.18). Bao *et al.* introduced polyimide (PI)[93] and silsesquioxane[94] resins as gate-dielectric materials. Klauk *et al.* demonstrated the first

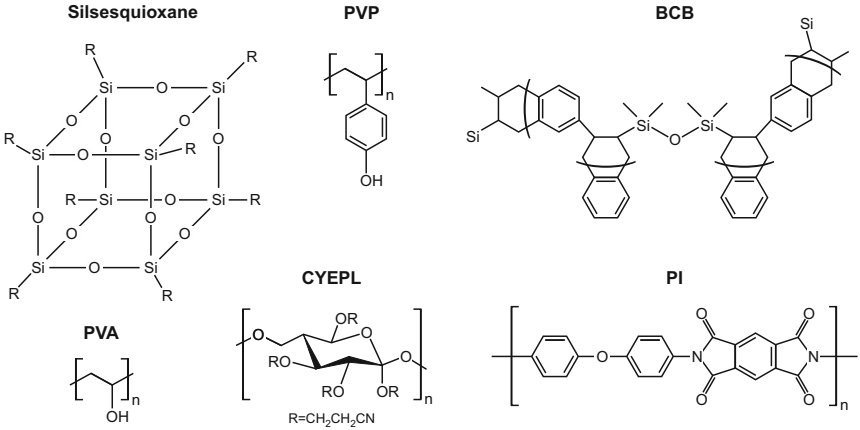

Figure 2.18. Structures of selected organic dielectrics. See text for details.

crosslinked polyvinylphenol (PVP; $k \sim 4$)[95] dielectric, which is later improved by others.[96–98] The first ultra-thin ($\sim$ 50 nm), pinhole-free dielectric films with high dielectric breakdown strength ($> 3\,\mathrm{MV/cm}$) and low leakage current ($< 10\,\mathrm{nA}$) were fabricated from thermal-crosslinkable divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB) by solution-casting.[99]

In general, polymer dielectrics are very attractive for OTFT applications due to their compatibility with plastic substrates. However, they mostly have low dielectric constants and film thicknesses below 1 µm are usually not functional due to high leakage currents. In order to get over these disadvantages, hybrid dielectrics which consist of inorganic-polymer bilayers have been proposed.[100–105] These hybrid dielectrics not only benefit from higher dielectric constants but also offer improved roughness of the dielectric layer. Another similar approach is to employ composite functional gate dielectrics, which are produced by dispersion of high-k inorganic nanoparticles such as barium titanate ($BaTiO_3$),[106–109] titanium dioxide (TiO_2)[110–114] in various polymers. However, obtaining a good dispersion of nanoparticles in the polymer matrix to reduce the leakage current through composite dielectrics is still a challenge. A more detailed information on dielectric materials for OTFTs can be found in review papers from Veres *et al.*[115] and Facchetti *et al.*[116,117]

2.2.2.3 Electrodes

An efficient charge transfer between the semiconducting layer and drain/source electrodes is crucial for proper OTFT operation. Therefore, the work function of the contacts should match with the conduction band or valence band of the semiconductor for n-channel or p-channel operation, respectively. Gold (Au) is frequently employed for p-channel operation due to its good hole injection properties into most organic semiconductors.[7] As a noble metal, Au is very stable in ambient atmosphere. Copper (Cu),[118–120] silver (Ag)[119,121] and platinum (Pt)[122,123] have also been reported as source/drain electrodes in OTFTs. On the other hand, low work function metals such as calcium (Ca),[124,125] barium (Ba),[126,127] and magnesium (Mg),[128,129] which favor electron injection into the LUMO energy level of some organic semiconductors, have been utilized for n-channel operation. Yet, these metals are instable and they oxidize quickly in case of ambient oxygen, which degrades OTFT device performance. Other non-noble metals, such as aluminum (Al) and chromium (Cr) have been employed for the gate electrode in bottom-gate device configurations, due to their good adhesion on various substrates, such as glass and plastic.[4] Indium tin oxide (ITO) is another gate electrode material, which–as one of the most widely used conducting oxides–can be structured on various substrates.[130] ITO is colorless and transparent to visible light, therefore, it is used as top electrode in many displays and light emitting/harvesting devices, such as organic light-emitting diodes (OLEDs) and organic photovoltaic (OPV) devices. Although the above mentioned electrode materials are not soluble, solution processable alternatives such as particle-based inks have been reported.[121,131]

Conducting polymers provide an alternative to metals and transparent conducting oxides. Polyaniline (PANI),[132] poly(3,4-ethylenedioxythiophene):poly (styrene sulfonic acid) (PEDOT:PSS),[133] polypyrroles (PPy)[134] have been successfully shown to form the source/drain electrodes in OTFTs. Since these polymers are soluble, they are of prior importance to achieve printable, all-organic OTFTs.

2.2.3 Fabrication

This section introduces with some brevity the techniques which are common for OTFT fabrication. Although the emphasis is given to the techniques which are used for the fabrication of the probes studied in this thesis, some other relevant

fabrication techniques are also briefly reviewed.

2.2.3.1 Substrate preparation

The operation of thin-film devices is strongly dependent on the quality of the thin sheets of functional materials which make up the device. Any irregularity or contamination on the substrate can physically or electrically disturb the functionality of the thin film which will be deposited on it. Therefore, substrate preparation is of prior importance for all thin-film applications.

An initial step of substrate preparation is surface cleaning, which can be divided into two main categories: dry and wet cleaning. Dry cleaning processes mostly employ gas phase chemistry in combination with annealing, sputtering and plasma etching. Wet cleaning, on the other hand, uses different solvents or acids to spray, scrub, etch and dissolve contaminants from substrate surface. Various solvents (e.g. acetone, chloroform) and acids (e.g. sulfuric acid, hydrofluoric acid, hydrochloric acid) as well as special mixtures such as piranha clean, i.e. sulfuric acid/hydrogen peroxide/deionized water, are used depending on the substrate (e.g. silicon, glass, plastic) and the kind of the surface contamination (e.g. plasticizers, hydrocarbons, particulates). The effect of wet cleaning can be improved at elevated temperatures in an ultrasonic bath.[135]

Another method to remove hydrocarbons from the substrate is the UV/Ozone treatment. In this process, the substrate is illuminated with a low-pressure mercury (Hg) lamp, which emits high-energy ultraviolet (UV) light at two specific wavelengths. The emission at the wavelength of 185 nm decomposes some ambient oxygen molecules into oxygen atoms, which react with other oxygen molecules to produce ozone (O_3).

$$\begin{aligned} O_2 + \text{photon}\ (UV\ @\ 185\,\text{nm}) &\longrightarrow 2\ O \\ O + O_2 &\longrightarrow O_3 \end{aligned} \tag{2.2}$$

The other emission wavelength at 254 nm decomposes O_3 into an oxygen molecule (O_2) and a high energy atomic oxygen (O^*), which is also called activated oxygen.

$$O_3 + \text{photon}\ (UV\ @\ 254\,\text{nm}) \longrightarrow O_2 + O^* \tag{2.3}$$

Activated atomic oxygen is very reactive and oxidizes the hydrocarbons on the substrate surface to form CO_2 and H_2O, which can be easily removed from the substrate. Oxygen supply into the process chamber and heating substrate

to elevated temperatures increases the produced ozone concentration and the hydrocarbon reaction speed, respectively.

Even in the case of contamination free substrates, the intrinsic properties of a surface may be inconvenient to grow the next functional layer on it or, alternatively, the interface between two functional layers may be inappropriate for an effective device operation. Surface modification through self assembled monolayers (SAMs) is an effective method to selectively engineer the condition of surfaces and interfaces. Molecules, which form the SAM, have a head, which attaches to the target substrate, and a tail, where the end group defines the new characteristics of the modified substrate. Since the head is designed to selectively attach to a certain material, a tightly packed, highly ordered and relatively robust single monolayer grows until all active sites on the substrate are occupied. It has been shown that modifying metallic contacts with SAMs improves the charge injection from electrodes into the organic semiconductor.[136,137] Other studies report that modification of the gate dielectric with SAMS in bottom-gate OTFTs leads to an increase in charge carrier mobilities due to the improved morphology of the organic semiconductor grown on the modified dielectric.[138,139]

2.2.3.2 Thin film deposition

An OTFT, as its name implies, consists of functional thin-films which are deposited on top of each other. Therefore, thin-film deposition constitutes an important part of OTFT fabrication. In the following various thin-film deposition methods are introduced, which we divide into two main groups according to the solubility of the functional material.

One of the simplest but powerful solution deposition methods is spin coating. It is realized by dispensing a solution of the target material onto a substrate, which is then rotated at its own central axis to spread the fluid by centrifugal force. It allows very precise control of the thickness down to several tens of nanometers and it can be applied to relatively large substrates. However, a post-processing annealing step is usually required in order to remove the solvent rest.

Drop-casting is a similar deposition method to spin coating. However, it is even simpler since the sample does not need to be rotated. Instead, the solution is dropped onto the substrate and a thin film forms as the solvent evaporates. The rate of solvent evaporation, which influences the morphology of the thin film, can be controlled either by using solvents with different vapor pressures

or by placing the sample in a chamber with a saturated solvent atmosphere. The thickness of the resulting film can be set through the concentration of the solution, however, it is neither uniform nor precise. Therefore, drop casting is usually utilized as a final deposition step, where no subsequent processing is required.

Thin-films can also be fabricated by dip coating, where the substrate is immersed into a solution and pulled up at a constant speed, where the excess liquid is optionally wiped with a blade. A significant advantage of this method is its ability to form uniform thin-films on curved and angled surfaces such as cylinders and prisms. A similar casting method is blade coating, where the solution is dispensed on a substrate and the excess liquid is wiped with a blade.

All solution deposition methods we have presented so far produce an unstructured thin-film which should be patterned in a further step. An alternative, where the thin-film is patterned during deposition, can be realized through printing techniques. The most used printing techniques can be listed as ejected drop printing (e.g. piezo or thermal inkjet), stream dispensing, contact stamp printing and offset printing. Beside the elimination of an extra patterning step, the advantages of printing techniques include more efficient use of source material and potentially high throughput through consecutive, roll-to-roll processes.

Although solution deposition is an effective low-cost fabrication method, not all of the materials used in OTFT fabrication are soluble. A fundamental deposition method, which can be used for insoluble materials, is the vacuum deposition. Depending on whether the source material only changes physical phase or it reacts chemically with other precursors to produce the desired deposit, vacuum deposition techniques can be classified into physical vapor deposition (PVD) and chemical vapor deposition (CVD), respectively.

One of the most popular PVD methods is the thermal evaporation which allows both purification and deposition of liquids and solids. The deposition occurs as molecules, which are removed from the source material through heating, condense on cooler target substrate. It is typically performed under high vacuum ($< 10^{-5}$ mbar) or ultra high vacuum ($< 10^{-9}$ mbar) conditions in order to minimize the contamination through ambient atoms and molecules. Another advantage of vacuum processing is the deflection free movement of source material in the absence of extrinsic molecules, such that a uniform thin-film grows on the target substrate. Another PVD technique, where higher deposition rates can be achieved is sputtering. In this method, with the help of an electric field, the

source material is bombarded with an ionized gas, which removes microscopic particles from the source material, which form a thin-film on the substrate. As process gas, an inert gas such as argon (Ar), neon (Ne) or xenon (Xe), which is ionized through a glow plasma discharge near the source material, is often preferred. The use of inert gases prevents unwanted chemical reactions between the source materials and the process gas. However, reactive gases can also be used to sputter compounds such as silicon dioxide (SiO_2),[140] aluminum nitride (AlN),[141] titanium carbide (TiC).[142] The most significant property of sputtering is the diffuse movement of source material to the substrate which does not allow a perfect patterning through shadow masks.

2.2.3.3 Patterning

In order to fabricate the different device geometries given in Fig. 2.14, it is necessary to pattern the thin-films which build up an OTFT. Patterning can be obtained additively as in the case of printing, where materials are selectively deposited. However, if a large area deposition technique is utilized, the deposited material needs to be removed at certain positions in a subtractive process to pattern the thin-film. Most patterning techniques employ a photolithography step, where a photosensitive material (usually called photoresist) is first deposited onto a substrate which is then illuminated through a photomask. Depending on the photoresist type, positive or negative, either the illuminated or non-illuminated sections of the photoresist can be washed away with a solvent to finalize the transfer of the desired layout onto the substrate.

One of the most popular subtractive patterning processes is etching, where the sections of different layers are chemically removed from the substrate. Depending on the type of the etchant, etching processes can be classified into liquid-phase (wet) and plasma-phase (dry) etching. Since etching is a large area process, it is usually used in connection with a photolithography step in order to define the sections to be etched. A similar process, which does not require any intermediate steps, is the laser ablation which can be used to remove the unwanted material in a direct write process. In this method, material is removed by irradiating it with a laser beam.

Lift off, on the other hand, is an additive patterning method where a sacrificial layer is patterned on the substrate through photolithography onto which the target material is deposited. The unwanted material is then lifted-off and removed with the sacrificial layer below, leaving the desired pattern on the sub-

strate. Shadow masking is another additive method which can be realized without photolithography. As the name implies, a mask which is kept near to the substrate blocks some of the deposited material, allowing it to reach to the substrate only at unshaded regions. It is an effective patterning method especially in connection with vacuum evaporation processes. However, complex layouts cannot be realized as the mask has to be self-supporting, which means no free-standing sections are realizable. Another limitation is the practically achievable feature size which is far below that of photolithography.

2.2.4 Electrical Characterization

In order to evaluate the performance of semiconducting devices, electrical characterization is essential. Among various approaches, monitoring the output and the transfer characteristics is the most established method to characterize field-effect devices. The former characteristics provide information on different operation regimes while the latter can be used to extract important OTFT parameters such as charge carrier mobility, threshold voltage, subthreshold slope, and on/off ratio.

Output characteristics show the dependency of drain-source current (I_{DS}) on drain-source voltage (V_{DS}) at a constant gate-source voltage (V_{GS}). For the measurement, V_{DS} is swept between a start and stop value while V_{GS} is kept constant. Then V_{GS} is changed and the V_{DS} sweep is repeated. A typical transient scheme of output characteristics measurement is illustrated in Fig. 2.19a. Transfer characteristics present the dependency of I_{DS} on V_{GS}. In contrast to the output characteristics, this time V_{GS} is swept while V_{DS} is kept constant. In order to investigate the phenomena such as hysteresis or threshold voltage shift, it is quite common in the literature that V_{GS} is swept cyclically. (Fig. 2.19b)

The operation of a field-effect transistor is essentially based on the capacitive coupling between the gate electrode and the semiconducting film. Therefore, in addition to the output and transfer characteristics, capacitance-voltage (C–V) characteristics provide supplementary information on field-effect device operation. C–V characteristics are usually measured from metal-oxide-semiconductor capacitor structures (see Fig. 4.1a) which we investigate in Chapter 4.

Two different approaches can be followed to measure the C–V characteristics. The first one, the conductance method, uses a small-signal AC signal superimposed on a DC offset (Fig. 2.20a). The small-signal current is measured which can be used to calculate the conductance of the probe. From the imaginary

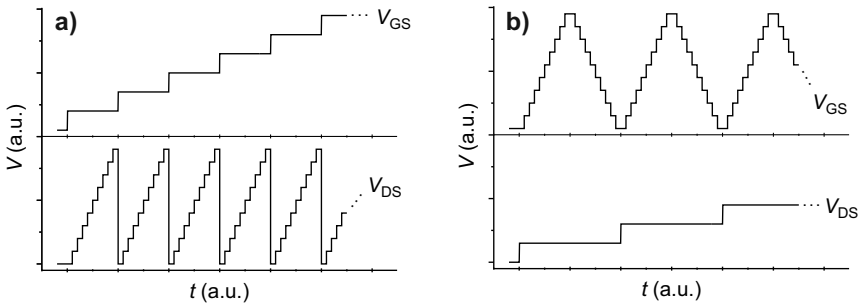

Figure 2.19. Typical transient schemes of (a) output characteristics measurement, where V_{DS} is the primary, V_{GS} is the secondary sweep parameter, (b) cyclic transfer characteristics measurement, where V_{GS} is the primary, V_{DS} is the secondary sweep parameter. a.u.: arbitrary units.

part of the complex conductance, the capacitance can be extracted. The significant advantage of this method is the fact that the measurement is unaffected from probable DC leakage currents since the small-signal displacement currents are monitored. Another advantage is the possibility to investigate the frequency dependency of the capacitance by changing the small-signal frequency. It is common to use frequencies between 10 kHz to 10 MHz for this purpose. However, low frequency measurements can also be performed.

Another method to monitor C–V characteristics–especially in low frequency range–is to perform quasi-static C–V (QSCV) measurements. This approach employs a slow ramp of DC voltage (ΔV) at different biases (Fig. 2.20b). During the volateg ramp, the current (I_{meas}) is measured and integrated over the ramp duration (Δt) to calculate the total amount of charge ($\Delta Q_{\mathrm{total}}$)

$$\Delta Q_{\mathrm{total}} = \int I_{\mathrm{meas}}\ dt. \tag{2.4}$$

Then, the capacitance can be calculated from

$$C = \frac{\Delta Q_{\mathrm{total}}}{\Delta V}. \tag{2.5}$$

If leakage current (I_{leak}) is present in the device, its contribution to the measured current should be subtracted. Then the net displacement charge (ΔQ_{dis}) caused by the applied voltage ramp reads

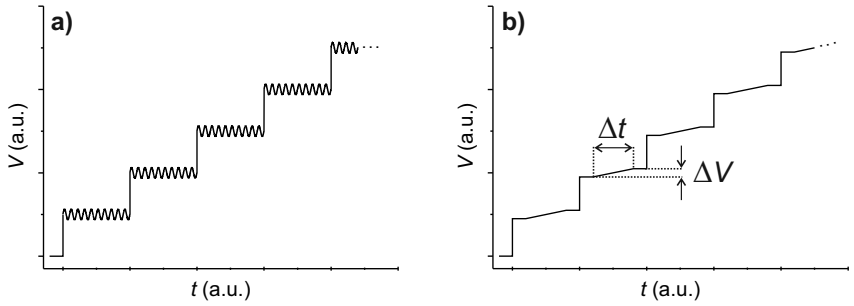

Figure 2.20. Typical transient schemes of (a) small-signal C–V measurement, (b) quasi-static C–V measurement.

$$\Delta Q_{\mathrm{dis}} = \Delta Q_{\mathrm{total}} - \Delta Q_{\mathrm{leak}} = \int (I_{\mathrm{meas}} - I_{\mathrm{leak}})\ dt, \tag{2.6}$$

which can be used to calculate capacitance, in accordance with (2.5), as

$$C = \frac{\Delta Q_{\mathrm{dis}}}{\Delta V}. \tag{2.7}$$

Chapter 3

Hysteresis in I–V Characteristics

A stable device operation is a key parameter for the reliability of electronic components. Organic thin-film transistors (OTFTs) are known to show operational instabilities, especially in form of alterations in the electrical device parameters. Such instabilities can be studied by monitoring the current-voltage characteristics. Provided that the time constants of the effects which lead to the instabilities are longer than the time required to perform an electrical measurement, e.g. the output (I_{DS} vs. V_{DS}) or transfer (I_{DS} vs. V_{GS}) characteristics measurement, transient shifts in the measured characteristics can be observed. This behavior, which leads to discrepancies in the measured I_{DS} values for repeated cyclic sweeps of V_{GS} or V_{DS}, is called hysteresis.

Hysteresis can be attributed to various effects which can be related to either the gate dielectric or the semiconducting film. Therefore, this chapter starts with a detailed literature survey on possible causes of hysteresis in OTFTs. Then we introduce our investigations on the hysteresis properties of hybrid OTFTs. Since our measurement results show a significant difference from those reported in the literature, we introduce a new model which relates the observed hysteresis in pentacene transistors to hole traps in the active layer. The validity of the proposed model is further investigated through numerical simulations with the two-dimensional device simulator ATLAS. Next, we introduce a behavioral OTFT model which can be used to simulate circuits with organic transistors. Finally, we investigate the impact of various measurement parameters on the I–V characteristics of OTFTs.

Parts of the results in this chapter have been published in Refs. [143–145].

3.1 A Literature Survey on Hysteresis in OTFTs

Mechanisms that cause hysteresis in Si-SiO_2 systems are already known for more than five decades and they are quite well described in the literature on inorganic field-effect devices.[84] For example, trapped charges at the semiconductor-oxide interface and charges (mobile, fixed or trapped) in the gate oxide have been reported to cause hysteresis in inorganic transistor devices.[146–150] If not all, most of these charges are also responsible for the hysteresis observed in OTFTs. In the following, different mechanisms that cause hysteresis in the I–V characteristics are discussed. These mechanisms, which are summarized in Fig. 3.1, can be categorized into two groups according to the location within the device, where they act.

3.1.1 Effect of Charges in the Semiconductor

Since the active channel forms within the semiconducting film, any charge in the semiconductor strongly influences the OTFT operation. In the next three subsections, we introduce the semiconductor-related mechanisms (illustrated with A1, A2, A3 in Fig. 3.1) which have been reported to cause hysteresis in OTFT characteristics.

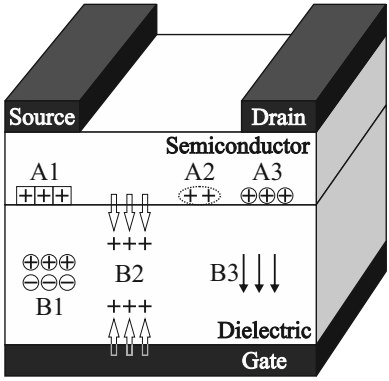

Figure 3.1. Scheme of a staggered, bottom-gate OTFT, illustrating the mechanisms that lead to hysteresis in the I–V characteristics. A detailed description of these mechanisms (A1-A3, B1-B3) can be found in the text. In general, each effect is independent of the sign of the charge. For the sake of simplicity, only holes are shown. Adapted from Ref. [10].

3.1.1.1 Traps (A1)

We have already mentioned in Chapter 2 that trap states are present in organic semiconductors. Both majority and minority charges can get trapped in these states. Once trapped, a charge cannot take part in charge conduction. Moreover, immobile trapped charges disturb the device operation by modifying the electric field within the accumulated channel. If the trapping rate and the lifetime of a trapped charge are comparable to the sweep rate of an electrical measurement, hysteresis can be observed in the device characteristics.

Gu *et al.* studied the trap states in a pentacene-based OTFT with a high quality, thermally-grown SiO_2 gate dielectric.[151] In order to explain the observed hysteresis in the transfer characteristics (Fig. 3.2a) with higher drain-source current (I_d) during OFF-to-ON sweep, i.e. the sweep from positive to negative gate-source voltages (V_{gs}) in case of p-channel operation, the authors introduced two possible explanations:

i) Hysteresis is due to deep electron traps in pentacene.[151] In presence of electron traps, which are filled during the OFF-state gate bias (i.e. at positive gate voltages), in addition to the holes which are induced by a negative gate bias, an excess of holes is induced in the channel to satisfy the charge-voltage relation. These additional holes increase the current during OFF-to-ON sweep. However, traps start to be emptied for the second half of OFF-to-ON sweep, i.e. at negative gate voltages, such that prior to the opposite gate bias sweep (i.e. ON-to-OFF), all electrons have already been released from traps due to the applied negative gate bias. Thus, with emptying traps the excess of holes disappears and there is no more positive contribution to the current during ON-to-OFF sweep, which leads to lower currents.

ii) Hysteresis is due to deep hole traps in pentacene.[151] At the beginning of OFF-to-ON sweep, hole traps are empty due to the positive gate bias. However, they are filled at negative gate voltages during the second half of OFF-to-ON sweep. Due to long trap lifetime, trapping of holes leads to "less mobile" holes, which cause the current to decrease during ON-to-OFF sweep.

In order to differentiate between these mechanisms, the authors performed time domain measurements (Fig. 3.2b).[151] Transistors were first biased at a range of initial gate-source voltages (V_{gs0}) for 100 s, which was followed by another 100 s

at $V_{gs} = -20\,\mathrm{V}$. It was observed that for positive initial gate biases, shown with empty symbols in Fig. 3.2b, I_d degraded after V_{gs} switch at $t = 0\,\mathrm{s}$. This can be explained with a decay in the trapped electron population in the second half of the measurement ($0\,\mathrm{s} < t < 100\,\mathrm{s}$). On the other hand, for negative initial biases, shown with filled symbols in Fig. 3.2b, I_d stayed constant when V_{gs} was switched to $-20\,\mathrm{V}$, since the electron traps had not been previously filled. The opposite should had been observed if hole traps were the cause of the observed phenomenon. Therefore, Gu *et al.* concluded that the hysteresis was caused by electron traps.

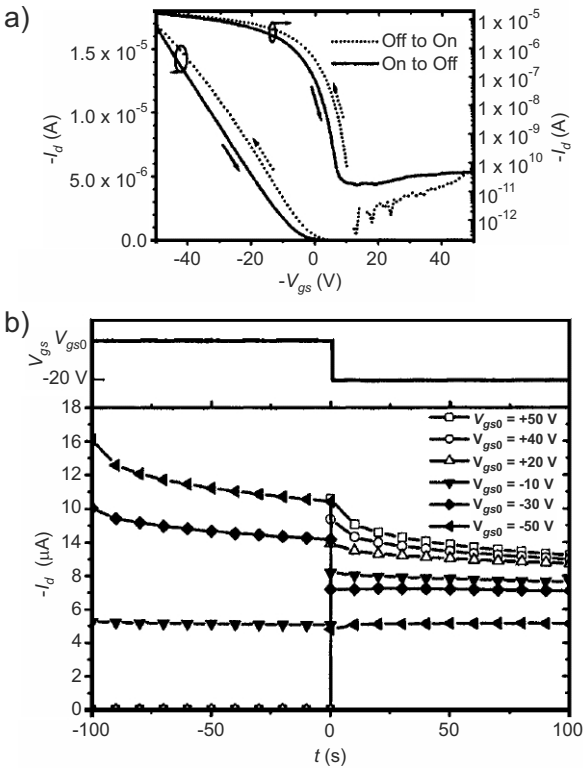

Figure 3.2. (a) Transfer, i.e. drain-source current (I_d) vs. gate-source voltage (V_{gs}), characteristics from a pentacene OTFT. (b) Transient I_d characteristics for the same transistor. The upper panel depicts the applied V_{gs} waveform and the lower panel shows the measured I_d data. Reprinted with permission from Ref. [151].

3.1.1.2 Slow reacting mobile charge carriers (A2)

The above mentioned fast trapping and slow detrapping of charge carriers leads to hysteresis which increases at higher sweep rates, i.e. the hysteresis is positively correlated to the sweep rate. However, it has been shown that decreasing the sweep rate can also lead to an increase in the hysteresis.[152] Simulations showed that a negative correlation between the hysteresis and the sweep rate cannot be explained with a trapping mechanism.[152, 153] Instead, slow reaction of mobile charge carriers has been suggested as an explanation for this kind of hysteresis.[154] Since charge carriers have more time to react to the applied bias at slower sweep rates, the hysteresis increases at lower rates and decreases at faster rates.

However, it should still be explained how slow reacting charge carriers arise. In Chapter 2, we have explained that polarons can overcome the coulomb repulsion and form doubly charged bipolarons. The mobility of bipolarons can be reduced by mobile counterions (e.g. charge impurities). Such interactions with counterions might stabilize bipolarons due to coulombic interactions and cause a hysteresis with negative sweep rate correlation.[153, 155] Another explanation is the slow rate of bipolaron formation, which is proportional to the square of polaron concentration.[154, 156]

3.1.1.3 Mobile ions (A3)

Mobile ions in the organic semiconductor can also lead to a hysteresis in the I–V characteristics. When a gate bias is applied, mobile ions in the semiconductor, which have the same polarity with the charge carriers that accumulate to form the conducting channel, move to semiconductor-dielectric interface. Since the total number of charges in the channel, which is determined by the gate bias and the capacitive coupling between the gate and the channel, is fixed, mobile ions reduce the number of charge carriers in the channel. Although, mobile ions can also contribute to charge conduction, they move much slower than the free charge carriers, which leads to a decrease in I_{DS} with increasing mobile ion concentration in the channel. Li and Na^+ ions in organic semiconductors are reported to cause this kind of hysteresis.[10]

3.1.2 Effect of Charges in the Dielectric

In an OTFT, the active channel forms in the semiconductor directly at the dielectric interface. Therefore, any charge in the dielectric, which is in the vicinity

of the accumulated channel, affects the distribution of charge carriers within the channel through coulombic interactions. Even the charges which are far away from the semiconductor interface influence OTFT operation by modifying the electric field across the dielectric, which is responsible for the channel formation. Consequently, reports on the effect of the dielectric on OTFT operation are frequent in the literature. In the following, we review three mechanisms (illustrated with B1, B2, B3 in Fig. 3.1) which lead to a hysteresis in the I–V characteristics of OTFTs.

3.1.2.1 Mobile ions (B1)

Mobile ions in the dielectric cause a hysteresis with higher currents during ON-to-OFF sweep in cyclic transfer characteristics. This effect is the opposite of that caused by mobile ions in the semiconductor, which we mentioned in the previous section. In case of a p-channel OTFT, if a negative gate bias is applied, the anions (negatively charged ions) move towards the semiconductor as the cations (positively charged ions) are attracted the gate electrode. The anions in the vicinity of the insulator-semiconductor interface attract holes and a channel is induced in the organic semiconductor. When gate bias is removed, ions do not redistribute immediately–since they cannot move fast–and keep their distribution for a while. This causes the channel to exist further and I_{DS} flows although the gate bias is removed, which leads to higher currents during ON-to-OFF sweep. Since the ions are moving slowly, decreasing sweep rate increases the hysteresis as more ions accumulate during longer application of the gate bias.

This kind of hysteresis is reported repeatedly in the literature for various dielectric-semiconductor combinations with more pronounced effects for OTFTs with organic dielectrics.[10] Movement of charged ions in poly(methyl methacrylate) (PMMA),[157] cyanoethylpullulane (CYEP),[158] poly-vinyl alcohol (PVA)[159] have been demonstrated to cause hysteresis in OTFTs.

3.1.2.2 Charges injected into the dielectric (B2)

Charges which tunnel from the organic semiconductor or the gate electrode into the dielectric can also cause hysteresis. If charges are injected from the semiconductor into the dielectric, the total number of mobile charge carriers in the channel, and therefore, I_{DS} decrease as long as ON-state gate bias is applied. The effect is similar to trapping of charge carriers in the semiconductor, such

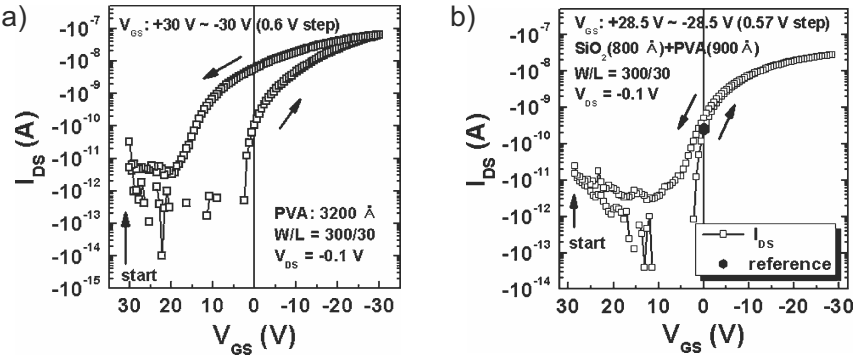

Figure 3.3. Transfer characteristics from a pentacene transistor with PVA gate insulator (a) without blocking thermal oxide, (b) with 800 Å blocking thermal SiO_2. Reprinted with permission from Ref. [163].

that ON-to-OFF gate bias sweep leads to lower I_{DS} than the other sweep direction.[160–162] On the other hand, if charges are injected from the gate electrode, the effect is similar to the mobile ions in the dielectric, such that injected charges in the dielectric cause the channel exist further after the gate bias is removed. As a result, a hysteresis with higher currents during ON-to-OFF gate bias sweep is observed.

If charges are injected from the gate electrode, hysteresis can be reduced through a blocking layer. For example, Lee *et al.* showed that by introducing a blocking oxide layer between gate electrode and poly-vinyl alcohol (PVA) gate insulator, the hysteresis in the transfer characteristics of a pentacene based OTFT can be reduced (Fig. 3.3).[163,164] Similar results have also been reported by others.[165–167]

3.1.2.3 Polarization of the gate dielectric (B3)

Polymer gate dielectrics can contain polar groups due to polar side groups, short polymer chains, residual solvents or incomplete cross-linking of the insulating polymer.[12,166,168] These polar groups align slowly with the external applied electric field and cause an additional gate field which leads to a hysteresis with higher currents during ON-to-OFF gate bias sweep. In a similar manner, ferroelectric dielectrics, which show remanent polarization due to an external electric field, cause the same kind of hysteresis.

The first application of ferroelectric material in OTFTs dates back to 2001.

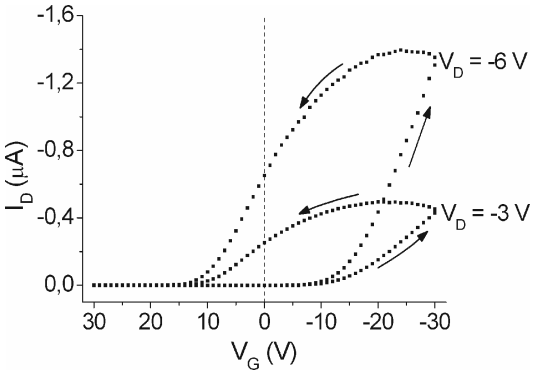

Figure 3.4. Transfer, i.e. drain-source current (I_D) vs. gate-source voltage (V_G), characteristics of a P3HT transistor with a ferroelectric composite layer of 10 vol. % barium titanate ($BaTiO_3$) content. Reprinted with permission from Ref. [108].

Velu *et al.* introduced the first ferroelectric OTFT based on an inorganic ferroelectric, Lead zirconate titanate (Pb(Zr, Ti)O_3), which is a solid solution of lead zirconate and lead titanate.[169] Other dielectric materials and approaches followed. Schroeder *et al.* demonstrated the first all-organic ferroelectric OTFT using a solution-deposited ferroelectric-like nylon gate insulator Poly(*m*-xylylene adipamide) (MXD6).[170] Naber *et al.* introduced poly(vinylidene fluoride/trifluoroethylene) (P(VDF/TrFE)) as an organic ferroelectric insulator to be used in ferroelectric OTFTs.[171] In order to improve ferroelectric properties, we have blended the copolymer (P(VDF/TrFE)) dielectric with barium titanate ($BaTiO_3$) nanopowder.[108] An enhanced hysteresis behavior with higher currents during ON-to-OFF sweep was observed (Fig. 3.4). All above mentioned efforts aim to engineer hysteresis to make it useful for certain applications, such as nonvolatile memory devices.

3.1.3 Effect of Extrinsic Factors

In the discussion given above, we have summarized the effect of intrinsic properties of organic materials on the hysteresis behavior. However, extrinsic factors such as temperature, light and ambient atmosphere (presence of oxygen or moisture) have also been associated to the hysteresis in OTFTs. It has been demonstrated that hysteresis related device instabilities are more pronounced in humid atmosphere than in vacuum.[172–175] This can be attributed to the moisture up-

take in the polymer dielectric which disappears upon annealing above 100 °C.[176] On the other hand, H_2O molecules can also diffuse in the organic semiconductor. In this case, the presence of moisture at the interface with the gate dielectric leads to hysteresis due to the large dipole moment of water molecules. Consequently, a reduced hysteresis was reported for OTFTs with SiO_2 gate dielectric, where dielectric surface was modified with hydrophobic self-assembled monolayers (SAM), which keep water molecules away from the active interface.[173,177] In contrast to humidity, oxygen undergoes a chemical reaction with thin films of acenes inducing trap states which lead to hysteresis. For example, as we mentioned in the previous chapter, pentacene is known to be highly reactive to oxygen at the two central carbon positions (6, 13).[25,49] Investigations on the effects of other extrinsic factors, such as temperature and light, on the hysteresis behavior have also been conducted.[159,174,178] Yet, these are likely to be a less general factor, which affects OTFT operation, than moisture.[9]

3.2 Experimental

Pentacene based hybrid organic thin-film transistors with inverted (bottom-gate) coplanar geometry (Fig. 2.14a) are utilized to investigate the I–V characteristics. Devices are fabricated on arsenic (As) doped silicon wafers (resistivity $< 0.005\,\Omega$cm) with a 300 nm thermally grown silicon dioxide (SiO_2) film which forms the gate electrode and the gate dielectric, respectively (Fig. 3.5). Wafers are delivered as front side polished (roughness < 2 nm) where the transistors are built. The drain and source electrodes are deposited from chromium (Cr) and gold (Au) through a shadow mask in Leybold vacuum deposition system. Using electron beam evaporation 5 nm Cr, which acts as an adhesion layer, and 40 nm Au are deposited in high vacuum ($< 10^{-6}$ mbar). Resulting electrodes have a dimension of approx. 2 mm × 3.5 mm with a 26 µm gap in between, which corresponds to a channel dimension of $W = 2$ mm, $L = 26$ µm. In order to eliminate surface contaminations, wafers are sonicated in ultrasonic cleaner first in acetone [$(CH_3)_2CO$] for 15 min, then in isopropanol [$(CH_3)_2CHOH$] for 5 min. They are rinsed with deionized water and dried on a hot plate prior to further processing. Bulk of n^+ doped silicon wafer forms the gate electrode of the transistor. In order to build the gate contact, SiO_2 is scratched on the front side and bulk silicon is contacted via silver (Ag) paste. In some cases, Au electrodes are also thickened with Ag paste, in order to minimize the possibility to damage the

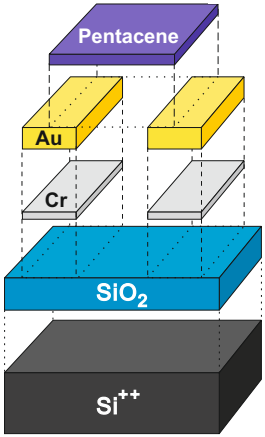

Figure 3.5. Fabrication scheme of inverted coplanar hybrid OTFTs. (not to scale)

underlying SiO_2 during device probing. During the later phases of the study, SiO_2 surface has also been processed with an ozone cleaner in order to remove organic contaminations more efficiently. Finally, a 50 nm to 120 nm thick pentacene layer is sublimed through another shadow mask to bring the active layer on Cr/Au electrodes. Pentacene (purity: 99.8 %) is purchased from Aldrich and evaporated as is at 1 Å/s in vacuum less than 10^{-5} mbar.

An Agilent precision semiconductor parameter analyzer (4156C) has been used for electrical measurements. During the measurements probes are kept in a glove box (MBraun MB 200B), which is a special bench designed to maintain a dry nitrogen (N_2) atmosphere with less than 0.1 ppm O_2 and 1 ppm H_2O. Transistors are probed with the help of a self-designed camera system which makes it possible to contact small electrodes properly. Different voltage ranges are swept on drain and gate electrodes using the programmable measurement function of the parameter analyzer, while the source electrode is kept grounded. At each step of the sweep function, drain, source, and gate currents are measured and recorded automatically. If it is not commented otherwise, an initialization routine, which is explained in the next section, has been executed prior to each measurement. For electrical characterization, output (I_{DS} vs. V_{DS}) and transfer (I_{DS} vs. V_{GS}) characteristics have been measured as introduced in the previous chapter (see Section 2.2.4). The parameters of the voltage sweeps used for I–V characterization are given in Appendix A.1.

3.3 Hole Trap Related Hysteresis

Output characteristics, which we have measured from a pentacene based organic thin-film transistor, are given in Fig. 3.6a. Since the injection of holes from the source electrode is more favorable than injection of electrons in our device configuration, i.e. with gold electrodes and pentacene as the active material, p-channel operation dominates, such that the transistor turns on for negative gate-source voltages (V_{GS}). Furthermore, linear and saturation operation regimes can be observed in accordance with (2.1) and Fig. 2.15. However, a clear hysteresis, which increases for faster sweep rates, is present in the characteristics (Fig. 3.6b). The hysteresis can also be observed in the transfer characteristics (Fig. 3.7).

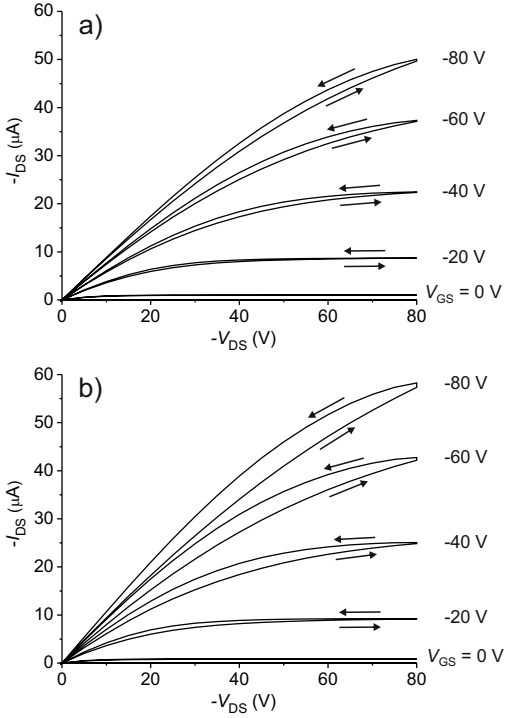

Figure 3.6. Output characteristics measured cyclically at different V_{DS} sweep rates from a pentacene OTFT with $L = 26\,\mu m$, $W = 2000\,\mu m$. V_{GS} is swept from 0 V to -80 V in -20 V steps. (a) Measured with slow V_{DS} sweep rate of 5 V/3 s. (b) V_{DS} sweep rate is increased to 5 V/50 ms. Hysteresis increases for faster V_{DS} sweep rates.

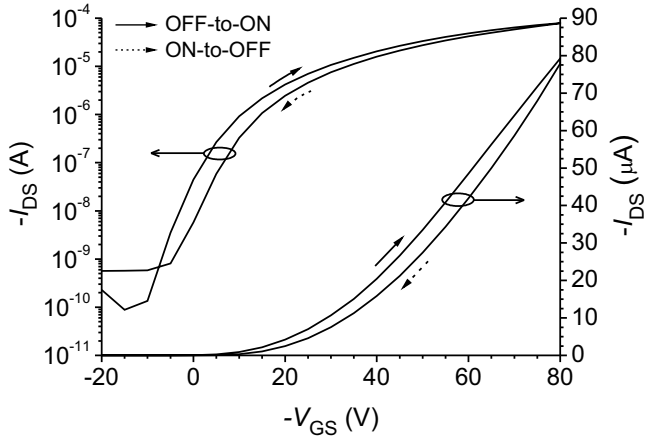

Figure 3.7. Transfer characteristics on linear and logarithmic scales measured from the same pentacene OTFT whose output characteristics are given in Fig. 3.6. V_{DS} is kept constant at -80 V as V_{GS} is swept between 20 V and -80 V in both directions. Higher currents flow during OFF-to-ON sweep. Reprinted with permission from Ref. [143].

In Section 3.1 we have explained that hysteresis in the transfer characteristics with higher currents during OFF-to-ON sweep compared to ON-to-OFF sweep can be related to the following mechanisms:

- Traps in the organic semiconductor,
- Charge injection from the organic semiconductor into the gate dielectric,
- Bipolaron formation in the organic semiconductor,
- Mobile ions in the organic semiconductor.

In the latter two cases, hysteresis is inversely proportional to the measurement time, i.e. slower voltage sweep rates should cause larger hysteresis loops due to the lower mobility of bipolarons and mobile ions than that of polarons.[10] However, this is not the case for our measurements (Fig. 3.6). Thus, one can conclude that either traps in pentacene or charge carrier injection into the gate dielectric or combination of these mechanisms leads to the observed hysteresis in our probes. However, hot carrier injection[34] from organic semiconductors into the SiO_2 gate dielectric is quite unlikely due to relatively low charge carrier mobility values (~ 1 cm^{2}V^{-1}s^{-1}) of organic materials and to our knowledge, it

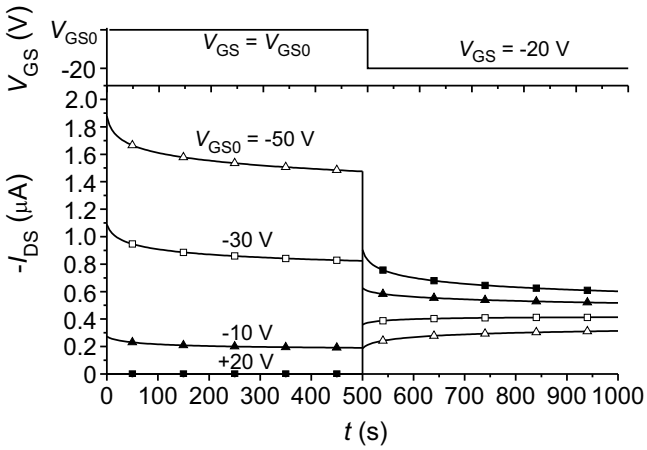

Figure 3.8. Drain-source current (I_{DS}) of a pentacene transistor is monitored for 1000 s, where gate-source voltage (V_{GS}), which is kept at an initial gate-source voltage (V_{GS0}), is switched abruptly to −20 V at $t = 500$ s. $V_{DS} = -10$ V. The measurement is repeated for different V_{GS0}, which is chosen in a range between 20 V and −50 V. Open symbols show the measurements where V_{GS} is switched to a less negative voltage at $t = 500$ s. Reprinted with permission from Ref. [143].

has not been previously reported. Therefore, we focus on traps in the organic semiconductor to investigate the observed hysteresis behavior.

In order to investigate what kind of traps are responsible for the observed hysteresis, we perform measurements to study the transient response of the transistors. For that purpose, gate-source voltage, which is kept at different initial gate-source voltages (V_{GS0}) for 500 s, is switched to −20 V and monitored for another 500 s (Fig. 3.8). V_{DS} is kept constant at −10 V. An initialization routine,[143] which we explain later in this section, is performed prior to each V_{GS0} change, in order to reset the probe to a defined initial state between subsequent measurements.

Measurement results in Fig. 3.8 show that the OTFT turns on and I_{DS} decays for the first 500 s when V_{GS} is switched to a negative voltage at $t = 0$. For $t > 500$ s, I_{DS} decays further if V_{GS} is switched to a more negative voltage (filled symbols) at $t = 500$ s, however it increases if otherwise (open symbols). In order to explain this behavior, we suggest a theory, which is based on trapping of majority charge carriers, i.e. holes, in pentacene. The theory is explained with the help of Fig. 3.9, which illustrates the transient behavior of a pentacene

OTFT during a gate voltage sweep, where V_{DS} is assumed to be set to a constant negative value. Figure 3.9a illustrates the charge and trap distribution in the semiconductor layer at various time points and gate biases, where Figs. 3.9b and 3.9c show the transfer and transient I_{DS} characteristics, respectively.

At $t = t_0$, a positive gate voltage ($V_{GS} = 20\,V$) is applied and the transistor is in OFF state. At this bias, holes cannot be injected into the organic semiconductor, thus there are no holes in the semiconductor and hole traps are empty. When V_{GS} is swept to a negative voltage, i.e. $V_{GS} = -40\,V$ at $t = t_1$, provided that $V_{GS} < V_{th}$, the gate field induces a conductive channel of accumulated holes at the dielectric-semiconductor interface and a hole current (I_{DS}) starts to flow between source and drain. However, when the semiconductor is flooded with holes, some of these starts to get captured by the existing trap states in the semiconductor ($t = t_2$). The trapping of holes decreases the free charge carrier density in the channel, which causes I_{DS} to decrease, as well. If V_{GS} is swept to a more negative voltage, i.e. $V_{GS} = -80\,V$, the hole density in the channel and I_{DS} increase at first ($t = t_3$), but then decrease again as more holes are trapped ($t = t_4$). On the other hand, if V_{GS} is swept to a more positive voltage, e.g. when it is swept back to $-40\,V$, I_{DS} first decreases with decreasing gate bias ($t = t_5$) but it increases in time as some captured holes start to get released from trap states ($t = t_6$). Thus, depending on the time constants of trapping/detrapping mechanisms, different device states can be observed although the device is biased identically. For example, at $t = t_6$, I_{DS} can be less than that at $t = t_2$ due to the higher number of trapped holes residual from V_{GS} sweep through $-80\,V$ (Figs. 3.9b, c). This explains why a hysteresis is observed in the transfer characteristics.

Trapping of holes in the channel explains the hysteresis in the output characteristics, as well. Holes, which are released with the decreasing vertical electric field near the drain at high negative V_{DS}, cause an increase in I_{DS} during backward V_{DS} sweep, i.e. when V_{DS} is swept to less negative voltages (Fig. 3.6). Therefore, compared to the hysteresis in the transfer characteristics, a hysteresis of reverse loop direction is observed in the output characteristics. Yet, measurements show that the sweep direction of V_{GS} still plays a role in the output characteristics (Fig. 3.10). Higher I_{DS} flows when V_{GS} is swept OFF-to-ON compared to ON-to-OFF sweep although V_{GS} is the secondary sweep parameter in output characteristics measurement. This is a clear indication that the time constants of trapping/detrapping mechanism is in the same range of the duration of typical I–V characteristics measurements.

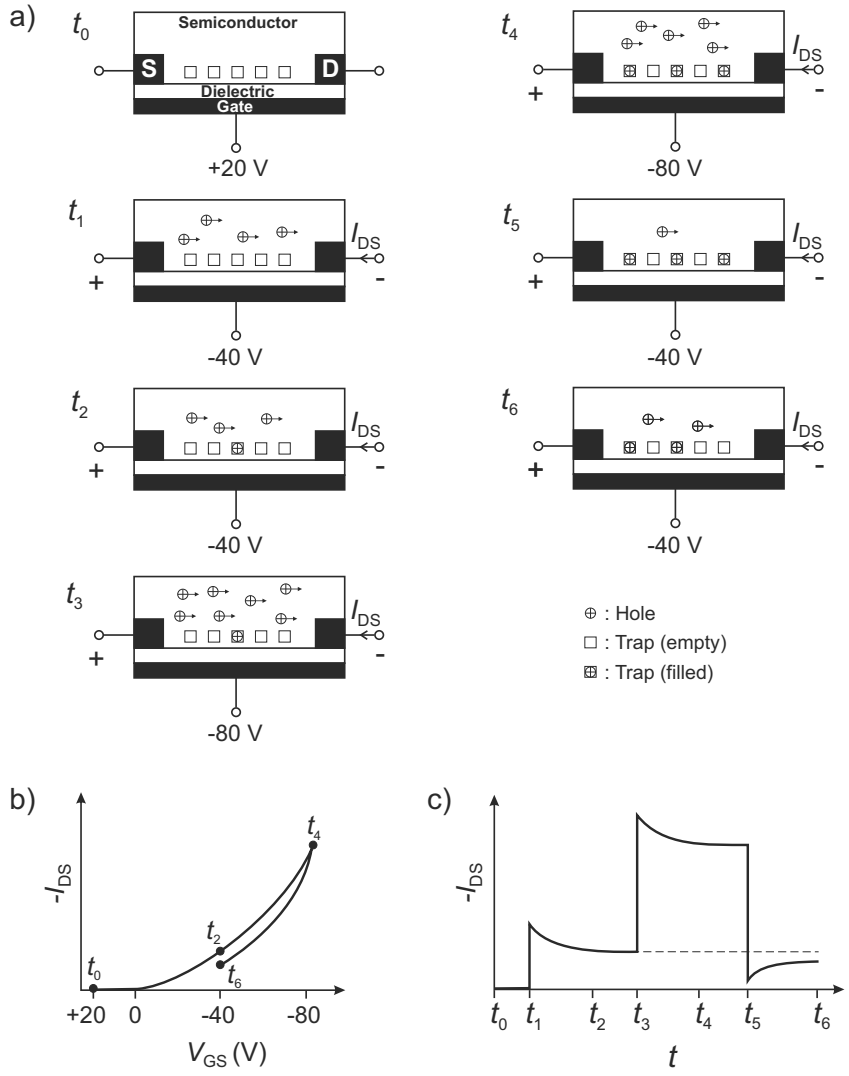

Figure 3.9. Transient behavior of a pentacene OTFT is illustrated during a gate voltage sweep. (a) Schematic cross-sectional view of the bottom-gate pentacene OTFT showing the charge carrier and hole trap distribution in the active layer during the sweep of the gate voltage (V_{GS}) from 20 V to −80 V and back to −40 V. (b) The resulting transfer characteristics and (c) transient I_{DS} behavior of the pentacene OTFT for the V_{GS} sweep depicted in (a). Adapted from Ref. [143].

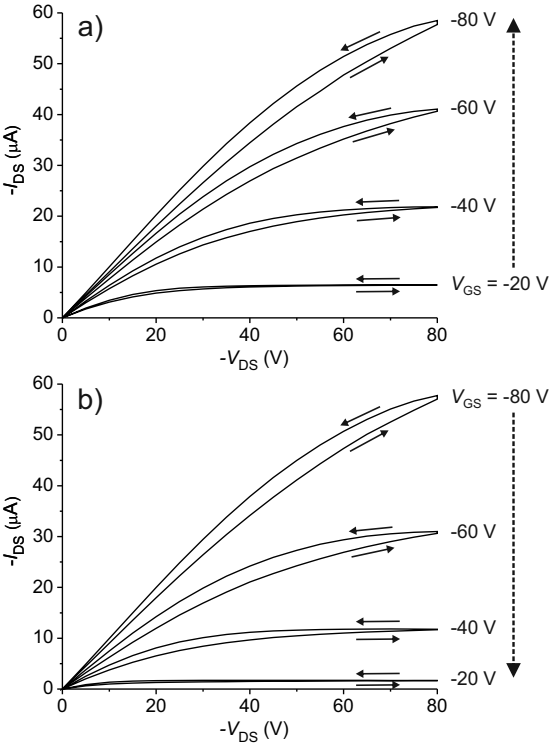

Figure 3.10. The effect of V_{GS} sweep direction on output characteristics measured from a pentacene OTFT. (a) V_{GS} is swept from 0 V to −80 V (OFF-to-ON) (b) V_{GS} is swept from −80 V to 0 V (ON-to-OFF). Waveforms for V_{GS} = 0 V are not visible as they lie on the horizontal axis. Solid arrows show the sweep direction of V_{DS} while dashed arrows show the sweep direct of V_{GS}. Reprinted with permission from Ref. [143].

In the following, we investigate the time constants of the trapping dynamics. Gu *et al.* have shown that the transient characteristics of I_{DS} at constant bias can be modeled with a second order exponential decay function as[151]

$$I_{\mathrm{DS}}(t) = I_0 + \mathrm{c}_1 \, \mathrm{e}^{\left(-\frac{t}{\tau_1}\right)} + \mathrm{c}_2 \, \mathrm{e}^{\left(-\frac{t}{\tau_2}\right)}. \tag{3.1}$$

We use the same approach to extract the time constants of the hysteresis mechanism. For this purpose, we fitted the measured transient characteristics in Fig. 3.8 with a second order exponential decay function, where the fit for $V_{\mathrm{GS}} = -50\,\mathrm{V}$ and $0 < t < 500\,\mathrm{s}$ is depicted as an example in Fig. 3.11. The time constants are extracted as $\tau_1 = 5\,\mathrm{s}$ and $\tau_2 = 140\,\mathrm{s}$.

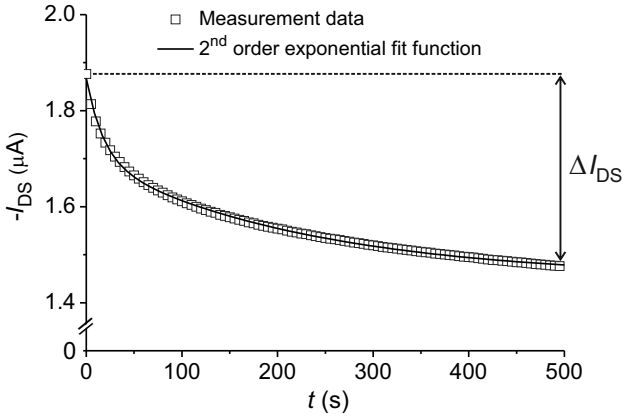

Figure 3.11. Transient I_{DS} curve from Fig. 3.8 for $V_{\mathrm{GS}} = -50\,\mathrm{V}$ and $0 < t < 500\,\mathrm{s}$ with a 2^{nd} order exponential fit function which can be used to extract the time constants of the trapping mechanism.

The above extracted time constants are so long that one should even consider, the trapping dynamics affect not only a single measurement but any subsequent measurements performed on the same device. In such systems it is almost impossible to perform reliable characterization with reproducible results since no two subsequent measurements are identical. In order to determine the impact of this effect on our devices, we perform transient measurements where the gate-source voltage is swept between two constant values repeatedly. Results given in Fig. 3.12a show that the current characteristics changes up to 10 % at higher

gate bias and up to 50 % at lower gate bias only after four measurement cycles. Therefore, in order to improve the reproducibility of the electrical characterization measurements, we propose an initialization routine to be utilized prior to measurements on OTFTs. Since the device instability is primarily due to the trapped holes in the active layer, a set of positive gate voltage and bias time is investigated to reverse the trapping mechanism. We report that a premeasurement stress for 50 s at $V_{GS} = 50\,V$, $V_{DS} = 0\,V$ significantly reduces the memory effects between subsequent measurements for the voltage range used for typical I–V characterization measurements. For verification, the transient measurement in Fig. 3.12a is repeated with the proposed initialization routine performed prior to each gate bias cycle. The results show that the OTFT characteristics become stable through initialization (Fig. 3.12b).

The distribution of traps states within the organic semiconductor is of particular interest. It is reported in the literature that charge traps on the semiconductor-dielectric interface is a possible cause of hysteresis in OFETs.[151,179–181] In order to investigate the role of oxide-pentacene interface on hysteresis, we have fabricated self-assembled monolayers (SAMs) on SiO_2 through hexamethyldisilazene (HMDS) vapor priming. Trimethyl siloxane (TMS) monolayer on the oxide surface not only favors the molecular ordering of the pentacene film grown but also eliminates possible structural disorders which act as traps.[182,183] The water-related trap formation is also eliminated due to the hydrophobic SiO_2 surface after the treatment.[173] Results, which are not given here, show that there is no significant change in the hysteresis characteristics of the transistors with and without HMDS treatment. Therefore, we comment that the dominant cause of the hysteresis in pentacene TFTs with SiO_2 gate dielectric cannot be solely related to the interfacial effects, but it should be a volume trapping effect.[184]

Finally, we perform a quantitative evaluation of the hole trap mechanism by calculating the trap density required to cause the observed hysteresis. Assuming a constant charge carrier density between the source and drain in the accumulation layer of an OTFT, I_{DS} for the linear regime can be calculated from

$$I_{DS} = \frac{W}{L} q\mu\sigma|V_{DS}|, \tag{3.2}$$

where W is the channel width, L is the channel length, q is the elementary charge, μ is the charge carrier mobility, and σ is the area density of the charge carriers in the channel.[151] Since the hole trap theory implies that the transient change in I_{DS} (ΔI_{DS}) at constant bias (see Fig. 3.11) is due to trapping/detrapping of

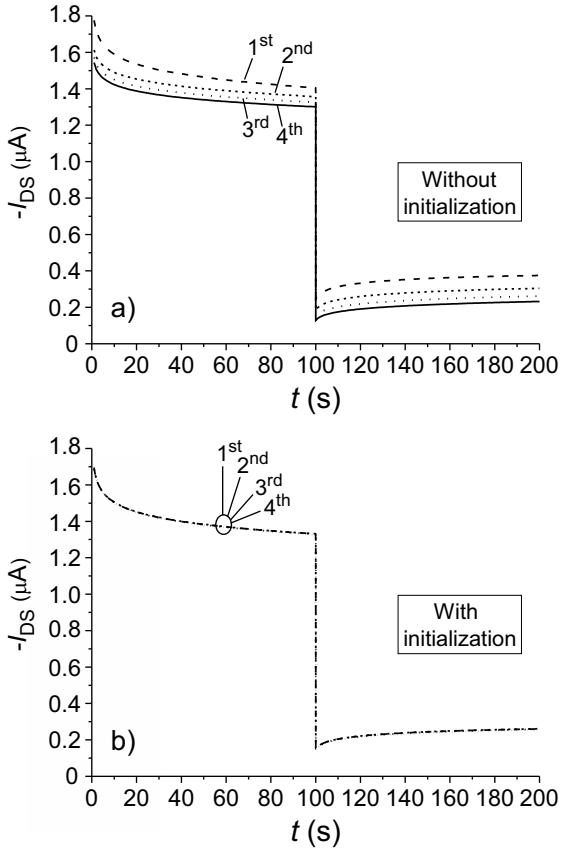

Figure 3.12. Drain-source current (I_{DS}) of a pentacene OTFT is measured for 1000 s, where gate-source voltage (V_{GS}) is switched from -50 V to -20 V at $t = 500$ s. $V_{DS} = -10$ V. (a) Measurements are performed successively without initialization. (b) A gate bias of $V_{GS} = 50$ V, $V_{DS} = 0$ V is applied for 50 s prior to each measurement. Reprinted with permission from Ref. [143].

holes which affects the free charge carrier density in the channel, we can write

$$\Delta I_{\mathrm{DS}} = \frac{W}{L} q\mu\sigma_{\mathrm{t}} |V_{\mathrm{DS}}|, \tag{3.3}$$

where σ_t is the area density of trap states, assuming all available traps are involved. Extracting the field-effect mobility (μ) in the linear regime from

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}}\right|_{V_{\mathrm{DS}}=\mathrm{const.}} = \frac{W}{L}\mu C'_{\mathrm{i}} |V_{\mathrm{DS}}|, \tag{3.4}$$

where g_{m} is the transconductance, and C'_{i} is the capacitance per unit area of the gate insulator, and inserting it into (3.3) yields

$$\sigma_{\mathrm{t}} = \frac{\Delta I_{\mathrm{DS}} C'_{\mathrm{i}}}{g_{\mathrm{m}} q}, \tag{3.5}$$

which is valid as long as V_{DS} is same for (3.3) and (3.5).

Reading $\Delta I_{\mathrm{DS}} = I_{\mathrm{DS}}|_{t=0} - I_{\mathrm{DS}}|_{t=500}$ from Fig. 3.11, σ_t is calculated from (3.5) as $2 \times 10^{11}\,\mathrm{cm}^{-2}$, which is almost an order of magnitude smaller than the trap density values given in the literature.[151, 179] A possible reason for the discrepancy is the assumption in our calculations that all traps in the pentacene are filled during the limited measurement time, which would actually require much longer measurements due to the long time constants of trapping/detrapping process. Without this assumption, the calculated value is the density of the trapped charge carriers, which is expected to be less than the density of traps states in pentacene. Consequently, the calculation justifies, to a good extent, the plausibility of the charge trap related hysteresis mechanism in pentacene OTFTs.

3.4 Simulations

In order to check the validity of the hole trap related hysteresis behavior of OTFTs, we have performed two-dimensional numerical simulations with the physical device simulator ATLAS from Silvaco. Simulations are performed for a device structure that corresponds to pentacene OTFTs on which the electrical measurements of the previous section have been conducted (Fig. 3.13). The thin chromium layer of 5 nm, which is necessary as an adhesive medium for the gold electrodes in the fabricated devices, has also been considered in the simulations although it has barely effect on the electrical behavior. For the pentacene layer, typical values have been chosen for the band gap (2.0 eV), the electron affinity

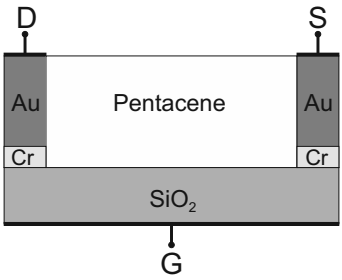

Figure 3.13. Schematic cross-section of the pentacene OTFT used for simulations (not to scale). Reprinted from Ref. [144] with permission from Elsevier.

(3.0 eV), and the relative permittivity (4.0). The effective density of states has been set equal to the density of molecules, i.e. $1 \times 10^{21}\,\mathrm{cm}^{-3}$.[185,186] Pentacene is assumed to be nominally undoped.

The hole mobility of $5 \times 10^{-3}\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ has been extracted from OFF-to-ON transfer characteristics of the fabricated devices for the voltage range relevant for the simulations. A Poole-Frenkel mobility model has been utilized in order to account for the electric field dependence of the charge carrier mobility. The hole Poole-Frenkel factor, β_p, has been calculated from the permittivity of pentacene.[187] The trap lifetimes of $\tau_1 = 5\,\mathrm{s}$ and $\tau_2 = 140\,\mathrm{s}$, which we have extracted from the transient behavior of the fabricated transistors, are used for simulations. In order to calculate the trap density, we have considered the spectral density of hole traps in the band gap of pentacene. Trap density of states (N_t) can be very well approximated by the exponential function

$$N_\mathrm{t}(E) = N_\mathrm{t0}\,\exp\left(-\frac{|E - E_\mathrm{t0}|}{E_\mathrm{S}}\right), \tag{3.6}$$

where N_t0 and E_S are the maximum and the characteristics width of trap density of states (DOS) in the bandgap, respectively, E_t0 is the energetic offset of the maximum of trap DOS from the valence band edge.[188,189] By integrating N_t over the band gap of pentacene, the volume density of hole traps can be calculated. Assuming hole traps to be concentrated at a discrete energy level of 0.1 eV above the HOMO edge, i.e. $E_\mathrm{t0} = 0.1\,\mathrm{eV}$, and using the typical values from the literature,[188] i.e. $N_\mathrm{t0} = 10^{20}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, $E_S = 0.1\,\mathrm{eV}$, a trap density of $2 \times 10^{19}\,\mathrm{cm}^{-3}$ is calculated and used in the simulations.

In order to investigate the role of charge trapping on the hysteresis behav-

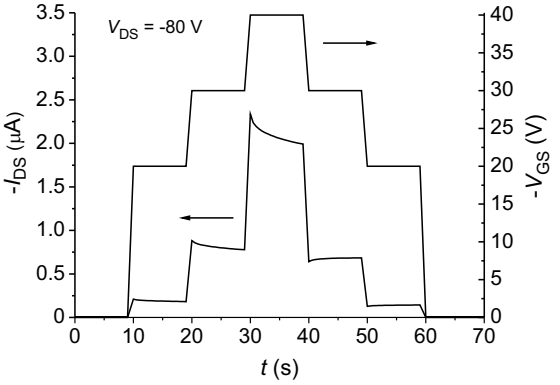

Figure 3.14. Measured transient I_{DS} characteristics of an OTFT in response to a V_{GS} sweep. At each V_{GS} step the bias is kept constant for 9 s and switched to next step with 10 V/s sweep rate. V_{DS} is kept constant at −80 V. Reprinted from Ref. [144] with permission from Elsevier.

ior, we perform simulations and compare them to the measured characteristics. For this purpose, first the transient response of I_{DS} at different gate biases is measured (Fig. 3.14). At each V_{GS} step the bias is kept constant for 9 s and switched to next step with 10 V/s sweep rate. V_{DS} is set to −80 V at $t = 0$ s and kept constant through the entire measurement. The previously mentioned characteristic, i.e. I_{DS} decreases transiently following a change in V_{GS} toward more negative voltages and vice versa can be recognized. Next, we simulate the measured characteristics with ATLAS. Parameters such as bias voltage, voltage sweep rate, and duration of the measurement are set exactly the same as in the measurement. The simulation results shown in Fig. 3.15a are in good accordance with the measurement.

In order to clarify the physical background of the transient change in I_{DS} during the measurement, we have also investigated the change in the trapped hole density in the active layer of the transistor. For this purpose, three consecutive time points are chosen in a time span in which the bias is kept constant. These are marked with letters A, B, C, which refer to $t = 30$ s, $t = 32$ s, $t = 38$ s, respectively (Fig. 3.15a). At these time points, the simulated trapped hole densities are shown on the cross-section of the transistor in Fig. 3.15b. In order to make the change at higher concentrations more remarkable, only the first couple of nanometers of the pentacene layer are shown and a linear scale is chosen be-

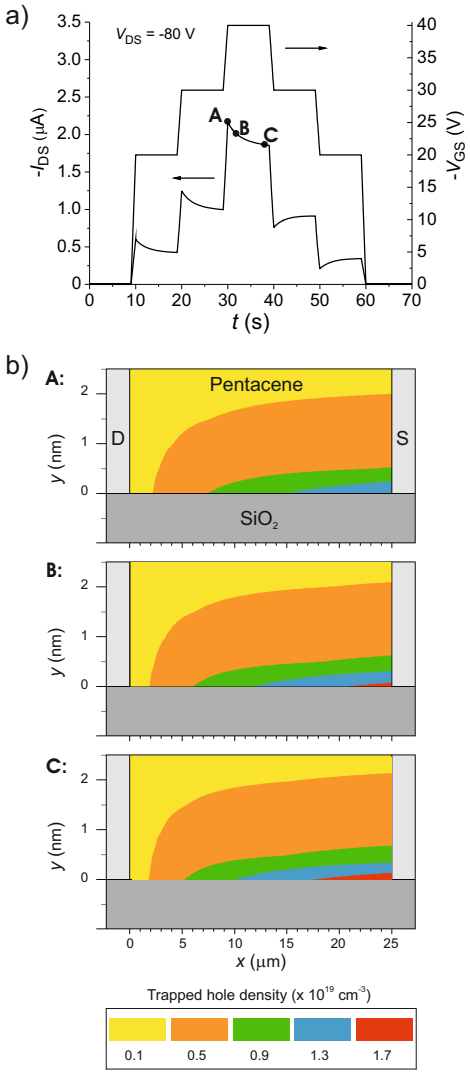

Figure 3.15. Simulations performed with ATLAS. (a) Simulation of the transient response of I_{DS} of a pentacene OTFT at different gate biases. (b) The density of trapped charge carriers (holes) in the channel at time points A: $t = 30\,s$, B: $t = 32\,s$, and C: $t = 38\,s$. The increase in the number of trapped holes in the channel is in accordance with the transient decay in I_{DS} for $30\,s < t < 38\,s$ shown in (a). Reprinted from Ref. [144] with permission from Elsevier.

tween $1 \times 10^{18}\,\mathrm{cm}^{-3}$ and $1.7 \times 10^{19}\,\mathrm{cm}^{-3}$ for the trapped charge carrier density. As the simulation advances, an increase in the trapped charge carrier density in the channel is observed (Fig. 3.15b). This increase in the number of trapped charge carriers reduces the number of effective charge carriers in the accumulation layer causing the transient decrease in I_{DS} for $30\,\mathrm{s} < t < 38\,\mathrm{s}$ in Fig. 3.15a. Thus, we conclude that the transient change in I_{DS} and hence the hysteresis can be explained by hole trapping in the active layer of OTFTs.

3.5 Behavioral Modeling

In electronics, modeling is an effort to implement some form of analogy to the electrical behavior of a device or a circuit. In addition to existing devices, modeling also offers the possibility to investigate hypothetical devices and circuits which have not yet been manufactured. Therefore, it prevents time consuming and expensive trial-and-error approaches. Semiconductor device modeling can be divided into two broad categories. "Physical device models attempt to incorporate the physics of device operation whilst equivalent circuit models are based on electrical circuit analogies representing the electrical behavior".[190] We used the latter approach to develop a compact behavioral OTFT model which takes into account the charge trapping related effects both in sweep and transient characteristics.

We have already seen that hysteresis in OTFTs can be observed both in the transfer and output characteristics (Figs. 3.6, 3.7). Hole trap related hysteresis theory postulates that hysteresis stems from a change in the number of available free charge carriers in the accumulation layer of the transistor. This change corresponds to a threshold voltage shift (ΔV_{th}) which can be observed in the transfer characteristics, at best. If we consider the saturation regime, V_{th} can be graphically read from $\sqrt{|I_{\mathrm{DS}}|}$ vs. V_{GS} plot where the linear extension of the plot intersects the voltage axis.[85] The threshold voltage shift during a cyclic transfer characteristics measurement is demonstrated in Fig. 3.16.

In order to develop a behavioral model for the observed hysteresis behavior, we use an approach which makes use of the above explained V_{th} shift. Since the I–V characteristics of OTFTs can be described, to a good extent, with the equations developed for MOSFETs, for the behavioral model we employ a standard PSpice MOSFET model but modify its V_{th} with respect to the applied bias. Since the trapping depends primarily on the gate bias, both gate-source

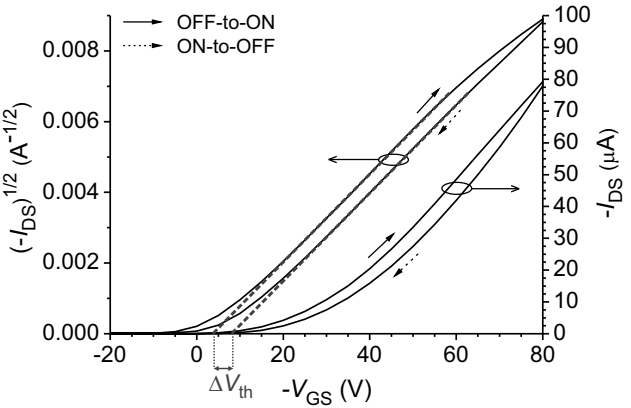

Figure 3.16. Measured transfer characteristics given in Fig. 3.7 replotted in a square root scale of I_{DS} against V_{GS}. The threshold voltage (V_{th}), which is determined from the intersection point of the linear fit (dashed lines) with the voltage axis, shifts during the measurement (ΔV_{th}).

(V_{GS}) and gate-drain (V_{GD}) voltages are considered. The different I_{DS} values for different voltage sweep directions is achieved by controlling ΔV_{th} through an RC network (Fig. 3.17). In order to improve the transient response of the model, we have used previously extracted trapping time constants of $\tau_1 = 5\,\mathrm{s}$ and $\tau_2 = 140\,\mathrm{s}$. Thus, two RC networks in parallel are used to realize τ_1 and τ_2, which are weighted with constants c_1 and c_2, where $0 < c_1, c_2 < 1$ and $c_1 + c_2 = 1$. Finally, as the dependency of I_{DS} on V_{th} is different for the linear and saturation regimes, a piecewise linear function ($\mathrm{f_{PWL}}$) is employed to adjust ΔV_{th} for different operation regimes. Further information on PSpice model parameters is given in Appendix B.1.

According to the model in Fig. 3.17, the output and transfer characteristics of a pentacene OTFT are simulated using PSpice and compared to the measured characteristics (Fig. 3.18a,b). In order to verify the transient response of the model, transient measurements are also simulated (Fig. 3.18c). Results show that the behavioral model is able to reproduce both sweep and transient characteristics of pentacene OTFTs including hysteresis effects.

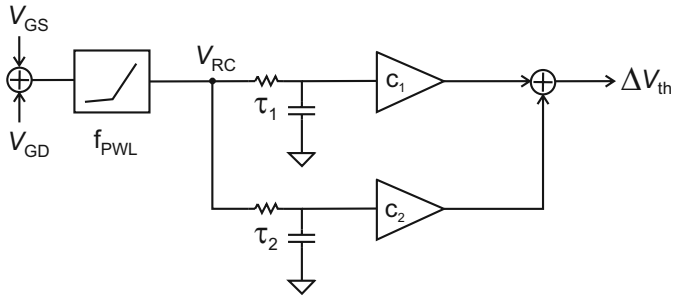

Figure 3.17. PSpice model which is used to control the threshold voltage of a standard MOSFET in order to develop a behavioral model for OTFTs regarding hysteresis. Reprinted from Ref. [145] © 2008 IEEE.

3.6 Impact of Measurement Parameters on Hysteresis

We have already demonstrated that hysteresis dynamics of OTFTs can exhibit time constants which are in the range of up to several hundred seconds. These long transients cause the response to an applied bias to be influenced by the device bias history. Although such kind of memory effects between subsequent measurement cycles can be prevented through initialization, as shown in Section 3.3, the trapping dynamics can still affect an ongoing measurement depending on the timing parameters of the measurement. Especially, in transfer and output characteristics measurements, where more than one parameter is swept consecutively, the impact may be significant since the time constants of hysteresis dynamics exceed the duration of a typical I–V characteristics measurement. Therefore, in this section we investigate the impact of electrical measurement parameters on hysteresis in standard I–V characteristics of OTFTs.

In I–V characteristics measurements, it is a good practice to introduce a time delay between the application of the test voltage and the reading of the current in order to prevent inaccurate or erroneous readings before the response of the device under test (DUT) settles. However, if not carefully chosen, the delay time can alter the measured I–V characteristics. In order to demonstrate the impact of delay time (t_{delay}) we refer to Fig. 3.19, where the transient response of I_{DS} at different gate-source biases and the resulting I–V characteristics are illustrated in accordance with the measurements presented previously in this chapter. In this example, V_{DS} is assumed to be set to a certain negative value

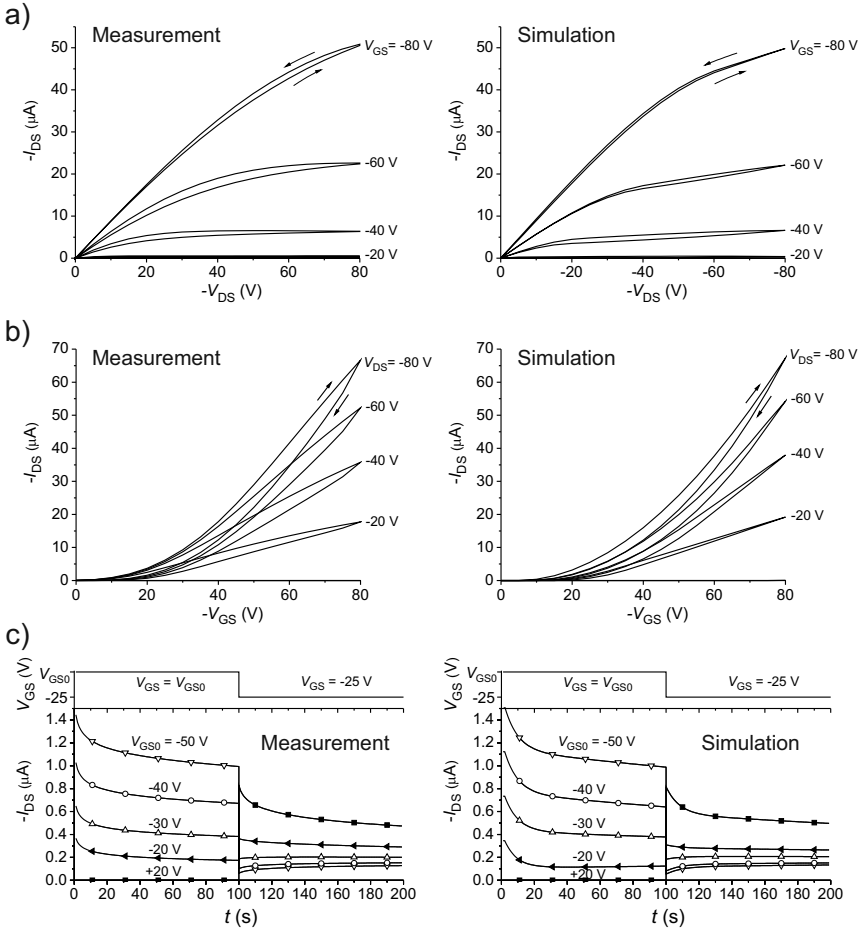

Figure 3.18. Measured and simulated characteristics for a pentacene transistor with $L = 26\,\mu m$, $W = 2000\,\mu m$. (a) Output characteristics. Arrows show the sweep direction of V_{DS}. (b) Transfer characteristics. Arrows show the sweep direction of V_{GS}. (c) Transient characteristics where gate-source voltage (V_{GS}), which is kept at an initial gate-source voltage (V_{GS0}), is switched abruptly to $-25\,V$ at $t = 500\,s$. Open symbols show the measurements where V_{GS} is switched to a less negative voltage at $t = 500\,s$. Reprinted from Ref. [145] © 2008 IEEE.

and kept constant through the entire measurement, while V_{GS} is swept from 0 V to a negative voltage for $t \leq t_2$ (OFF-to-ON) and then back to 0 V for $t \geq t_3$ (ON-to-OFF). For the sake of simplicity, only one intermediate V_{GS} step is considered for each sweep direction. i.e. $V_{\mathrm{GS}}|_{t=t_1}$ for OFF-to-ON and $V_{\mathrm{GS}}|_{t=t_3}$ for ON-to-OFF (Fig. 3.19a). In order to constitute the transfer characteristics from the transient characteristics two different sets of consecutive measurement points with different delay times, i.e. t_{delay} and $t_{\mathrm{delay}'}$, are chosen, which are marked with letters A, B, C and A′, B′, C′, respectively (Fig. 3.19b). The resulting I–V characteristic from the first set of measurement points (A, B, C) with shorter delay time t_{delay} is given in Fig. 3.19c, while the characteristic from the second set of measurement points (A′, B′, C′) with the longer delay time $t_{\mathrm{delay}'}$ is given in Fig. 3.19d. Although a hysteresis with the same rotational direction is present in both characteristics, the width of the hysteresis becomes smaller with increasing delay time.

In order to demonstrate the impact of measurement parameters on output characteristics, we refer to Fig. 3.20, where the transient response of I_{DS} at different drain-source biases and the resulting I–V characteristics are illustrated. In this example, V_{GS} is assumed to be set to a certain negative value and kept constant throughout the measurement, while V_{DS} is swept from 0 V to a negative voltage and then back to 0 V to extract the output characteristics. The critical measurement parameter concerning the output characteristics is the hold time (t_{hold}). It is the amount of waiting time in nested sweep measurements between the application of the secondary and the primary sweep variable, i.e. V_{GS} and V_{DS}, respectively, in output characteristics.

First, we investigate the case when t_{hold} is long enough such that the transient of the gate bias related effects can be neglected and only the change in V_{DS} influences the current I_{DS}. Under this assumption, the transient behavior of I_{DS}, which is depicted with a solid line on the right hand side of Fig. 3.20b, can be explained as follows. Following a V_{DS} sweep to more negative voltages, I_{DS} increases transiently as the number of available charge carriers increases due to detrapping at the drain end of the channel. In contrary, during the other sweep direction, I_{DS} decreases following a change in V_{DS} as the charge carriers are trapped when the effective electric field at the drain edge of the channel increases with decreasing drain bias. Thus, the output characteristics shown in Fig. 3.20d, interpolated from the measurement points marked with letters A, B, C in Fig. 3.20b, show the same hysteresis behavior with the previously presented

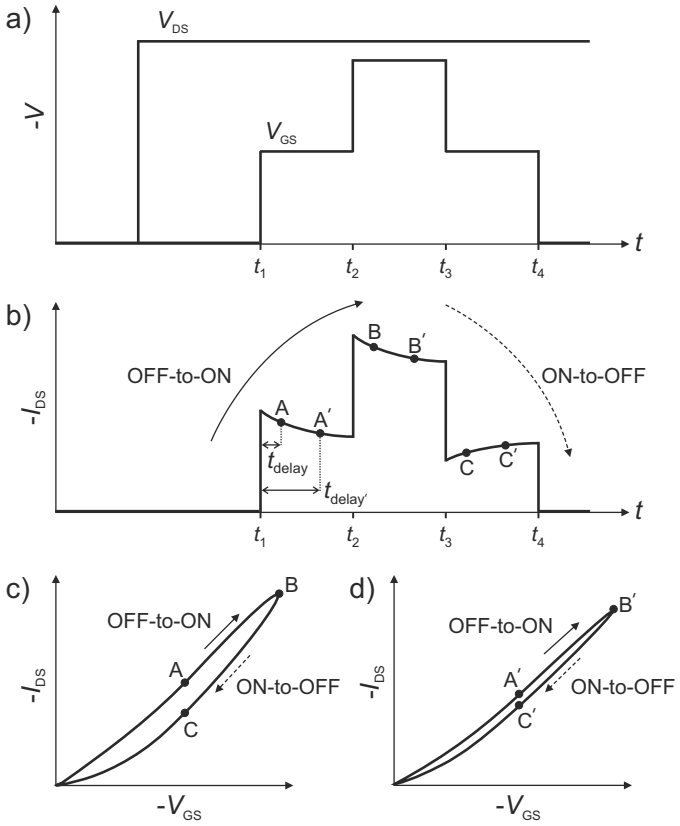

Figure 3.19. Illustration of the transient response of I_{DS} during the transfer characteristics measurement of an OTFT. (a) Successive steps of drain and gate biases. (b) Transient response of I_{DS}. (c) Transfer characteristics for shorter delay time t_{delay} interpolated from measurement points A, B, C. (d) Transfer characteristics for longer delay time $t_{delay'}$ interpolated from measurement points A′, B′, C′. Hysteresis width decreases with increasing delay time. Reprinted from Ref. [144] with permission from Elsevier.

output characteristics in Fig. 3.10, i.e. hysteresis with higher currents when V_{DS} is swept to less negative voltages (backward sweep).

The above explanation of hysteresis in output characteristics is only valid in case of a long hold time (t_{hold}). If the same V_{DS} sweep is applied with a shorter hold time ($t_{hold'}$), as depicted with dashes in Fig. 3.20a, the effects of the V_{GS} step at the beginning of the measurement overlap with those of the consequent V_{DS} sweep. Concerning hysteresis, the transient effects of drain and gate bias sweeps are contradictory. Yet, regarding the effect on the strength of the electric field in the channel, hence, the trapping dynamics, gate bias predominates since it affects the field strength in the whole channel area while the drain has an influence limited to its vicinity. Consequently, in case of a short hold time ($t_{hold'}$), the transient characteristics of I_{DS} - shown with dashes on the left hand side of Fig. 3.20b - are similar to the case for the transfer characteristics given in Fig. 3.19b. Consistently, the rotational direction of hysteresis in the output characteristics interpolated from the measurement points A′, B′, C′ is opposite of that of the characteristics extracted from the points A, B, C (Fig. 3.20c,d).

In order to figure out the impact of the hold time (t_{hold}) on device characteristics, output characteristics, measured with different t_{hold}, are investigated. For the sake of simplicity, the output characteristic is measured at a single gate bias, i.e. $V_{GS} = -80\,V$. V_{DS} is swept from $0\,V$ to $-80\,V$ and then back to $0\,V$ with $5\,V/s$ sweep rate. A delay time of $1\,s$ is introduced to achieve stable measurements. An initialization step, which is introduced previously in this chapter, is utilized between subsequent measurements. Nevertheless, the measurements are repeated with different sequences to verify that the results are free of long term degradation. The output characteristic measured with $t_{hold} = 30\,s$ exhibits a hysteresis with higher currents during the backward sweep (Fig. 3.21a). This is the case where the effects of the V_{GS} change at the beginning of the measurement can be neglected since t_{hold} is long enough to ensure that V_{GS} dependent effects settle during t_{hold}. However, with decreasing t_{hold}, the rotational direction of hysteresis in the output characteristic tends to change such that the forward and backward characteristics intersect (Fig. 3.21b). This is due to the fact that the gate and drain bias related hysteresis effects are contradictory and gate bias dependent hysteresis appears in the output characteristic as t_{hold} becomes shorter. The shorter the hold time, the more dominant is the gate bias dependent hysteresis and the intersection point in the characteristic moves toward more negative V_{DS} values (Fig. 3.21c). Thus, depending on the measurement parameters, it is

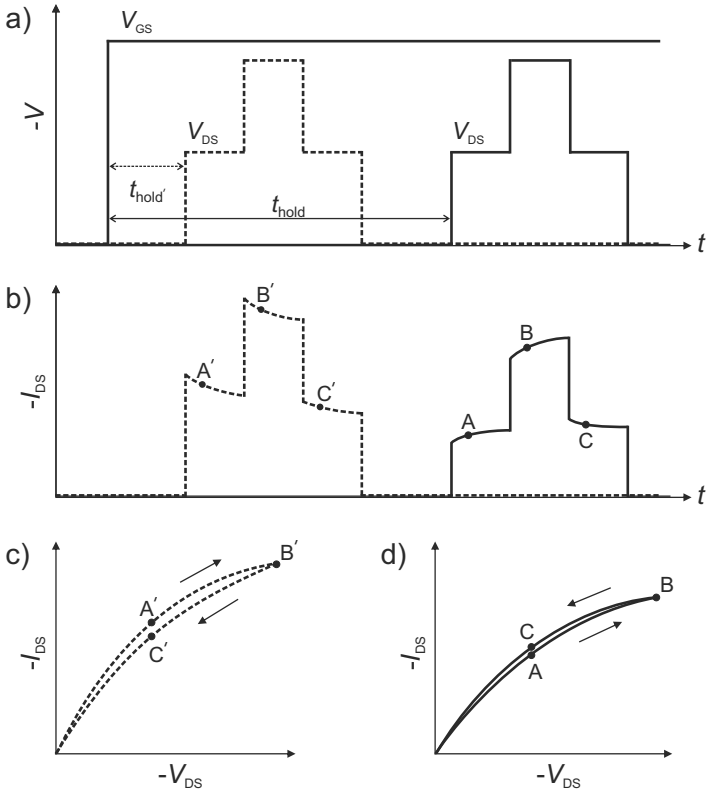

Figure 3.20. Illustration of the transient response of the channel current I_{DS} during output characteristics measurement with two different hold times, t_{hold} and $t_{hold'}$. (a) Time sequences of gate and drain biases. Wave form of V_{DS} for t_{hold} is shown with solid line and for $t_{hold'}$ with dashed line. (b) Transient responses of I_{DS}. Solid line for t_{hold}, dashed line for $t_{hold'}$. (c) Output characteristics interpolated from measurement points A′, B′, C′. (d) Output characteristics interpolated from measurement points A, B, C. The rotational direction of the hysteresis switches depending on the hold time. Arrows show the sweep direction of V_{DS}. Reprinted from Ref. [144] with permission from Elsevier.

possible to have contradicting rotational directions of hysteresis in the output characteristics as illustrated in Fig. 3.20. Furthermore, it can also be seen in Fig. 3.21 that the maximum value of I_{DS} decays with increasing t_{hold}.

3.7 Conclusions

In this chapter, we have presented a detailed study on hysteresis behavior in the I–V characteristics of pentacene-based OTFTs. For this purpose, in addition to the output and transfer characteristics, transient characteristics of OTFTs have been investigated. Since the theories in the literature cannot thoroughly explain the measured characteristics of our fabricated devices, we have introduced an alternative theory, which is based on hole traps in the organic semiconductor pentacene. The validity of the hole trap theory is demonstrated through measurements and device simulations, where the time and bias dependencies of the hysteresis have been investigated. Furthermore, we have extracted the effective time constants of the trapping mechanism as $\tau_1 = 5\,\mathrm{s}$, $\tau_2 = 140\,\mathrm{s}$ and the area density of traps as $\sigma_t = 2 \times 10^{11}\,\mathrm{cm}^{-2}$, which are in the range of the values given in the literature.

Due to the long time constants of trapping mechanism, it is a challenge to perform reproducible measurements on pentacene OTFTs. Therefore, we have introduced an initialization routine to be performed prior to measurements, which enables reproducible and reliable measurements. Yet, measurement results depend strongly on measurement parameters. We have demonstrated that solely by changing the hold time and/or the delay time in the measurements, it is possible to change the width and even the rotational direction of the hysteresis. Therefore, we conclude that it shall be a routine to comment on the electrical measurement parameters such as hold time, delay time, voltage sweep rate in all reports concerning OTFT characteristics.

Last but not least, we have introduced a behavioral model, which can reproduce both voltage sweep and transient characteristics of pentacene OTFTs including hysteresis effects. Due to its simple implementation in PSpice, the model can be combined with other OTFT models in order to introduce hysteresis response. Moreover, the model is not limited to the hole trap related hysteresis but can be used to model any type of hysteresis, which is related to a threshold voltage shift.

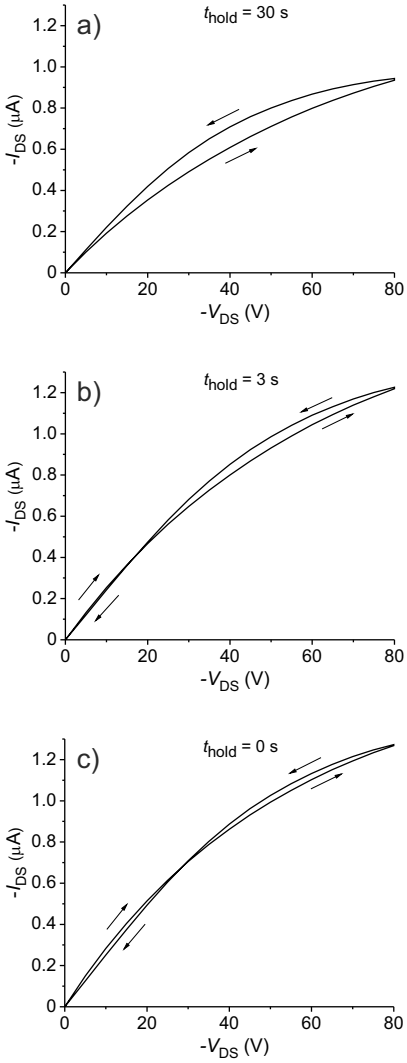

Figure 3.21. Output characteristics of a pentacene OTFT measured with different hold times (t_{hold}). $V_{\mathrm{GS}} = -80\,\mathrm{V}$. Gate bias dependent effects dominate in measurements with shorter t_{hold} causing a change in the rotational direction of the hysteresis. Arrows show the sweep direction of V_{DS}. Reprinted from Ref. [144] with permission from Elsevier.

Chapter 4

Hysteresis in C–V Characteristics

The operation of thin-film field-effect transistors is essentially based on a capacitive coupling between the gate electrode and the semiconducting film. Therefore, in addition to output and transfer characteristics, studying capacitance-voltage (C–V) characteristics is fundamental to understand the field-effect device operation.[34,191] Moreover, C–V characteristics can be utilized to investigate, for example, the doping concentration and profile in the semiconductor, charges and mobile ions in the gate dielectric and charges at the interface in between. Hence, C–V investigations constitute an important tool to study hysteresis related effects which we have introduced in the previous chapter.

Investigations on the C–V characteristics of OTFTs are rare in the literature. Nevertheless, this chapter starts with a short literature survey to introduce previous efforts. After explaining the experimental details on the fabrication of metal-oxide-semiconductor capacitor structures, we present the C–V characteristics of these structures. The characteristics include a plateau unlike the characteristics reported so far. We investigate the possible causes of this phenomenon through device simulations with ATLAS. Finally, we introduce a behavioral PSpice model which can be utilized to simulate the quasi-static C–V characteristics of organic transistors and capacitor structures.

Parts of the results in this chapter have been published in Ref. [192].

4.1 A Literature Survey on C–V Characteristics of OTFT Structures

Investigations on C–V characteristics have been generally conducted on metal-insulator-semiconductor capacitor structures. Since oxides are frequently used as the insulating material, these structures are called metal-oxide-semiconductor (MOS) capacitors (Fig. 4.1a). The equivalent circuit of a MOS capacitor is given in Fig. 4.1b, which consists of the oxide capacitance (C_{ox}) and the semiconductor capacitance (C_{sc}) in series such that the MOS capacitance (C_{MOS}) reads

$$C_{\mathrm{MOS}} = \frac{1}{\frac{1}{C_{\mathrm{ox}}} + \frac{1}{C_{\mathrm{sc}}}} = \frac{C_{\mathrm{ox}} C_{\mathrm{sc}}}{C_{\mathrm{ox}} + C_{\mathrm{sc}}}. \tag{4.1}$$

C_{ox} is the geometrical capacitance of the oxide layer which can be calculated from

$$C_{\mathrm{ox}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} A}{d}, \tag{4.2}$$

where ε_0 is the permittivity of the vacuum, ε_{r} is the relative permittivity of the oxide, d is the oxide thickness, and A is the area of the metal capacitor plates. As it can be seen in (4.2), C_{ox} depends only on the device geometry and the relative permittivity of the insulating material, thus, it is independent of the applied bias. C_{sc}, on the other hand, strongly depends on the bias as the charge distribution within the semiconductor changes with the applied bias, which is explained below. Therefore, C_{MOS} also depends on the applied bias.

In the following C–V characteristics of inorganic and organic MOS capacitors are introduced. For the sake of brevity, we focus on the low-frequency character-

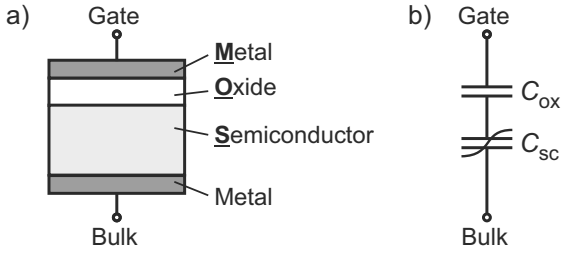

Figure 4.1. (a) Schematic cross-section of a metal-oxide-semiconductor (MOS) capacitor. (b) Equivalent circuit of the MOS capacitor is a series combination of the bias-independent oxide capacitance (C_{ox}) and the bias-dependent semiconductor capacitance (C_{sc}).

istics, which are relevant for the quasi-static C–V characteristics investigations performed in this thesis. In case of inorganic semiconductors, three different regimes can be observed in the low frequency C–V characteristics of MOS capacitors (Fig. 4.2a). For a p-type semiconductor, majority charge carriers (holes) in the semiconductor will be attracted to the oxide interface at a negative gate bias ($V_{\mathrm{GB}} < 0$), such that the hole density at this interface will greatly exceed the hole density in the bulk semiconductor. This regime is called accumulation and the measured capacitance is equal to the oxide capacitance (C_{ox}) since the charge carriers at the oxide interface respond to gate bias changes (Fig. 4.2c A,B). If the gate bias is made positive ($V_{\mathrm{GB}} > 0$), holes are repelled from the oxide interface into the semiconductor bulk and a depletion layer of ionized doping atoms (acceptors) forms (Fig. 4.2c C). As the gate bias becomes more positive, the depletion layer widens into the semiconductor bulk decreasing the measured capacitance since the charge carriers which respond to gate bias changes are further away from the gate electrode (Fig. 4.2c D). This regime is called depletion. If the gate bias is made even more positive ($V_{\mathrm{GB}} \gg 0$), the hole density at the semiconductor-oxide interface decreases whereas the electron density increases in according with the mass-action law, i.e. $pn = n_{\mathrm{i}}^2$, where p is the hole density, n is the electron density, and n_{i} is the intrinsic charge carrier concentration at the thermal equilibrium. When the surface electron density exceeds the surface hole density, an inversion layer of electrons is formed at the semiconductor-dielectric interface (Fig. 4.2c E). From now on these electrons respond to gate bias changes, therefore, the measured capacitance is once again equal to the oxide capacitance for any higher bias (Fig. 4.2c F).

The C–V characteristics of a MOS capacitor with an organic semiconductor is similar, yet not the same (Fig. 4.2b). In contrast with the depletion and inversion layers that form in inorganic semiconductors, electron or hole accumulation layers have been observed in organic semiconductors, where these charge carriers have to be injected from electrodes which are in contact with the organic semiconductor. Since the energy gap between HOMO and LUMO levels of most organic semiconductors are high ($\sim 2\,\mathrm{eV}$), depending on the work function of the contact metal, injection of one type of charge carrier dominates at moderate bias. For example, in case of a low energy barrier between the contact metal work function and the HOMO level of an organic semiconductor, holes will be injected and accumulate at the dielectric interface at a negative gate bias ($V_{\mathrm{GB}} < 0$). Then, the capacitance will be equal to the oxide capacitance (C_{ox})

as explained above (Fig. 4.2d A). As the bias becomes less negative, holes are no longer strongly attracted to the dielectric interface and the capacitance decreases, which corresponds to the depletion regime in inorganic semiconductors (Fig. 4.2d B). When the bias changes to positive ($V_{\mathrm{GB}} > 0$), the organic semiconductor is initially free of mobile charge carriers since the injected holes have been repelled away from the semiconductor and the electrons cannot be injected due to the unfavorable energy gap. Due to the low intrinsic charge carrier concentrations in organic semiconductors, inversion does not take place in organic MOS structures. Thus, the capacitance remains at its minimum value for even higher positive biases (Fig. 4.2d C, D, and E). Yet, depending on the energy gap of the organic semiconductor, at very high positive biases ($V_{\mathrm{GB}} \gg 0$), it is theoretically possible that electrons can also be injected into the organic semiconductor. Then, these electrons accumulate at the dielectric interface and the capacitance increases once again to the geometrical capacitance C_{ox} (Fig. 4.2d F).

One of the first investigations on C–V characteristics of organic structures was reported by Scheinert *et al.* who studied small-signal and quasi-static C–V curves for MOS capacitors with undoped and iodine-doped arylamino-poly-phenylene-vinylene (arylamino-PPV).[193] Measurements were performed on an Au/PPV/SiO_2/n^+-Si capacitor, where arylamino-PPV was spin-coated and dried under ambient atmosphere on a highly doped silicon wafer with thermally grown oxide layer. The Au contact is evaporated onto the organic layer through a shadow mask. The cyclic small-signal C–V curves for different frequencies between 1 Hz and 20 Hz showed a large hysteresis (Fig. 4.3a), which was also observed in the quasi-static C–V curves (Fig. 4.3b). Furthermore, a shift in the quasi-static curves was noticed for subsequent measurement cycles. The authors concluded that the observed C–V characteristics stem from unintentional p-doping of pristine arylamino-PPV and calculated a doping concentration of $2 \times 10^{16}\,\mathrm{cm}^{-3}$. They also calculated an interface charge carrier density of $2 \times 10^{12}\,\mathrm{cm}^{-2}$ to explain the shift of the flat band voltage in the characteristics.

Quasi-static C–V curves were further investigated for MOS capacitors with iodine-doped arylamino-PPV for various temperatures (Fig. 4.3c) and voltage ramp rates (Fig. 4.3d). From non-monotonous change of the hysteresis and shift of the curves with increasing temperature and ramp rates, the authors concluded that the observed effects could not be caused solely by a single mechanism but by a combined effect of different processes with different time constants. In

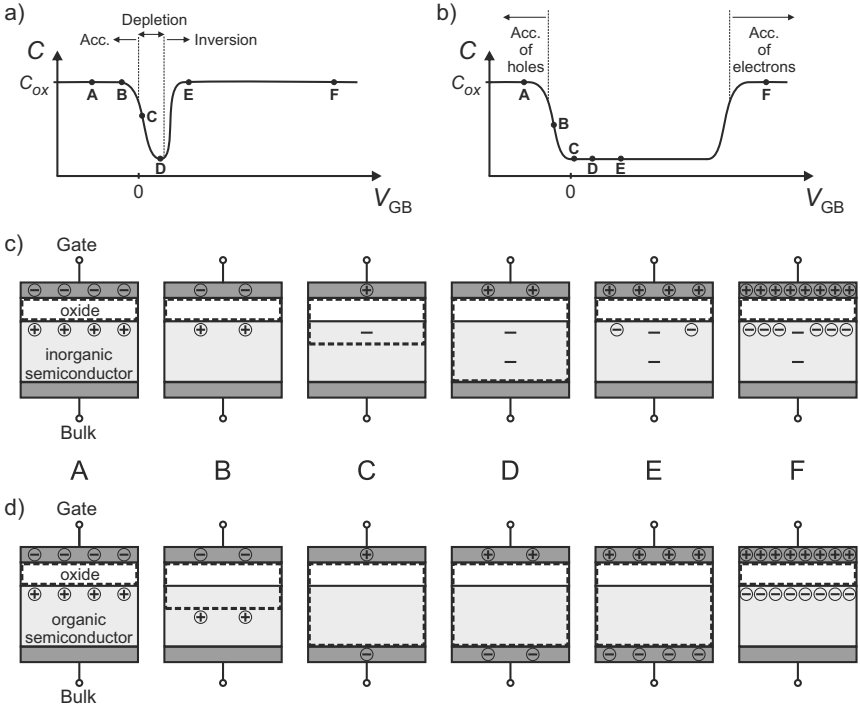

Figure 4.2. Illustration of the low-frequency C–V characteristics of a MOS capacitor with (a) p-type inorganic semiconductor (b) organic semiconductor. Various operation regimes are marked with arrows (Acc.: accumulation). Schematic view of the mobile charge carrier distribution within the MOS capacitor with (c) inorganic semiconductor (d) organic semiconductor. Capital letters (A to F) refer to different gate-bulk voltages (V_{GB}) in the C–V characteristics in (a) and (b). The dashed rectangle shows the separation of plates of the effective capacitance referring to a parallel plate capacitor. The mobile charge carriers are shown with plus (hole) and minus (electron) in circles. The ionized acceptor atoms in the depletion region of the inorganic semiconductor are shown with minus symbols without circles in (c).

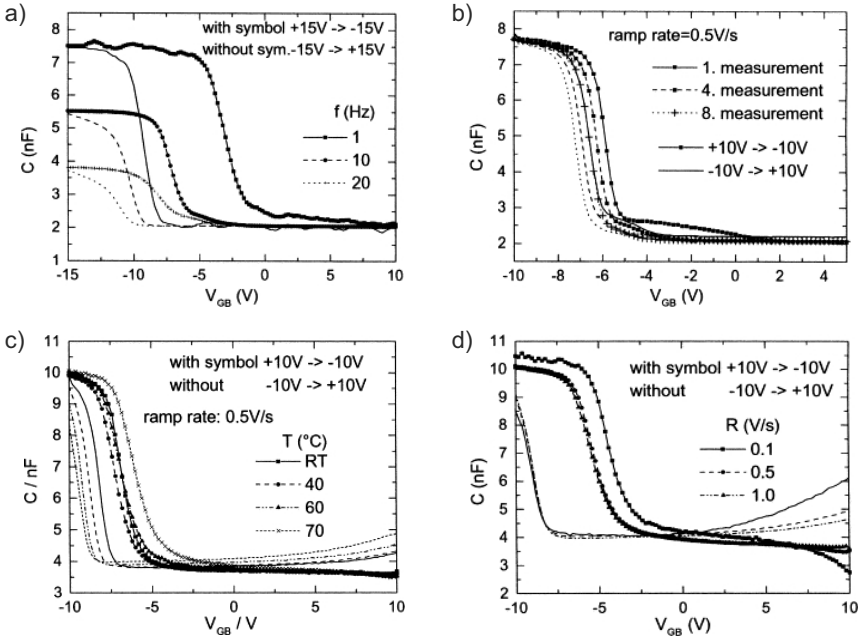

Figure 4.3. C–V curves of a MOS capacitor. (a) Dynamic C–V curves for different frequencies and sweep directions and (b) quasi-static curves for subsequent cycles of the MOS capacitor with an undoped layer. Quasi-static C–V curves of iodine-doped MOS capacitor for different sweep directions at different (c) temperatures and (d) ramp rates. Reprinted from Ref. [193] with permission from Elsevier.

further studies with Poly(3-octylthiophene) based MOS capacitors and through numerical simulations of QSCV characteristics of organic MOS structures, this group speculated that the main origin of hysteresis in organic devices should be a combination of slow transport (polaron or mobile ions) with a reaction other than trap recharging.[152, 153, 194] They proposed a direct polaron-bipolaron reaction or a complex formation reaction of polaron/bipolarons with counterions as a coexisting mechanism. This was, to some extent, contradicted by Yang *et al.* who reported a shift of the flat-band voltage in small-signal C–V characteristics of a pentacene-based MOS capacitor, which was correlated solely to the trapped charges at the dielectric-semiconductor interface.[195]

Chen *et al.* investigated bottom-gate coplanar pentacene OTFTs fabricated on a glass substrate where ITO was sputtered to form the electrodes and SiO_2

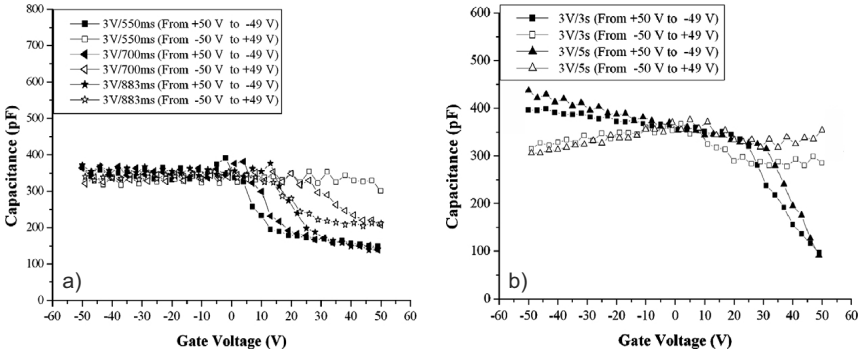

Figure 4.4. QSCV curves for a pentacene OTFT measured between the gate and electrically shorted drain and source electrodes for various gate voltage ramp rates (a) between 3 V/550 ms and 3 V/883 ms (b) at 3 V/3 s and 3 V/5 s. Reprinted from Ref. [196] with permission from Elsevier.

was coated by PECVD as the dielectric layer.[196] They measured the QSCV characteristics directly from the OTFT structure by connecting the drain and source together to form one plate of a capacitor while the gate formed the other plate. In order to lessen the impact of instability issues, before the QSCV characterization, samples were kept in box purged with dry air and monitored for longer than 80 days until the day-to-day variation of the I_{DS}–V_{DS} curves dropped below 5 %. The authors investigated various C–V curves with voltage ramp rates between 3 V/33 ms and 3 V/5 s and noticed a trend with decreasing hysteresis for decreasing voltage ramp rates (Fig. 4.4a), which was attributed to the difference in trapping and detrapping time constants of the pentacene film. A skew in QSCV curves was observed for lower ramp rates than 3 V/3 s, which was related to low-mobility carriers such as mobile ions or impurities that can follow the gate signal at these low ramp rates (Fig. 4.4b). No significant change in the C–V characteristics of transistors with different channel lengths was reported. In a similar study Kim *et al.* investigated the intrinsic capacitance characteristics of a top-contact pentacene-based polystyrene-gate OTFTs on glass, where the authors showed that the frequency-dependent capacitance can be modeled using an RC network.[197]

Lim *et al.* investigated the hysteresis behavior of inverted staggered pentacene-based OTFTs with Au source and drain electrodes and SiO_2 gate dielectric.[180] The authors electrically shorted the drain and source electrodes to measure the

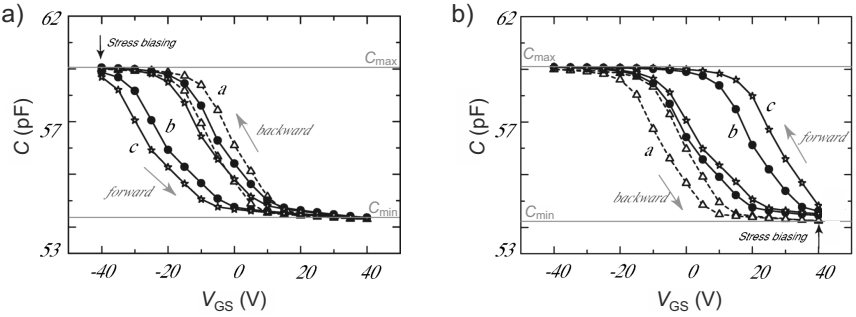

Figure 4.5. C–V characteristics measured with an AC frequency of 2 kHz after stress-biasing at (a) $V_{GS} = -40$ V, and (b) $V_{GS} = 40$ V. Stress-biasing times were 0 min (curve a), 10 min (curve b) and, 30 min (curve c). The scan direction is indicated by arrows for the forward and backward sweeping directions. Reprinted from Ref. [180] with permission from American Institute of Physics.

small-signal C–V characteristics (Fig. 4.5). Prior to the measurements, stress gate voltages of $V_{GS} = -40$ V (Fig. 4.5a) and $V_{GS} = 40$ V (Fig. 4.5b) are applied for 0, 10 and 30 min. It was shown that the hysteresis behavior depends not only on stress biasing time but also on the scan direction. The authors commented that the hysteresis is due to trapped charge carriers within the semiconductor and the shift of the threshold voltage is dependent on the amount of trapped charges. Through optical second generation harmonic (SGH) measurements, the charge injection from electrodes into pentacene was also examined. The authors detected trapped electrons in the semiconductor near the Au source and drain electrodes and concluded that the hole injection process is assisted by trapped electrons, which explains the increase in capacitance at positive gate biases in Fig. 4.5b for the forward sweep direction in curves b and c.

Furthermore, Ryu *et al.* studied the C–V characteristics of pentacene OTFT to propose a new method to extract the charge carrier mobility.[198] The authors presented the difficulty of extracting OTFT mobility by using the linear region MOSFET model especially when the I–V curves exhibit hysteresis. QSCV measurements were used to calculate the sheet charge density within the channel, and I–V measurements were used to extract the mobility. Gelinck *et al.* studied the conductance method and showed that it is possible to model the impedance data with a simple transmission line equivalent to calculate the small-signal C–V behavior for zero drain bias of an OTFT as long as the device geometry and QSCV characteristics are known.[199] Akhtaruzzaman *et al.* investigated small-signal

C–V characteristics of pentacene based MOS capacitors to study the hysteresis and air stability issues.[200]

The studies summarized above have been mostly conducted either on an OTFT with electrically short-circuited source and drain terminals, which contradicts the electrical configuration during normal transistor operation, or on a MOS structure given in Fig. 4.1a which neglects the channel region of an OTFT, i.e. the semiconductor film between the source and drain electrodes. Therefore, Jung *et al.* suggested C–V characterization to be performed on a MOS capacitor with a peripheral semiconductor region, which represents the active channel region of an OTFT (Fig. 4.6a).[201] The authors showed that the overall capacitance of this modified capacitor structure (C_{tot}), hence the capacitance of a staggered OTFT, can be considered as the sum of three different capacitances: the insulator capacitance (C_{i}), metal-semiconductor overlapping capacitance (C_{ov}), and the peripheral semiconductor region capacitance (C_{p}) (Fig. 4.6b). The C–V characteristics of these capacitances and the overall capacitance are shown in Fig. 4.6c.

Tanaka *et al.* used a similar approach to perform C–V characterization on pentacene OTFTs.[202] Instead of short-circuiting the source and drain electrodes, the bias was applied between the gate and one of these two electrodes while the other was left electrically floating. Results given in Fig. 4.7 show different maximum capacitance values depending on the measurement frequency. Tanaka *et al.* related this behavior to a difference of speed between the injection of charge carriers into the organic semiconductor and the spreading of them along the organic semiconductor-insulator interface. The authors claimed that the injected holes do not spread instantaneously along the semiconducting film due to the difference of the electric potential just under and far from the injecting electrode. Therefore, at high frequencies ($f > 1\,\mathrm{kHz}$) only a low capacitance (C_{inj}) can be measured, which stems from the limited charge accumulation just under the injecting electrode. However, at low frequencies ($f < 10\,\mathrm{Hz}$), the injected holes have enough time to spread along the whole semiconductor film, such that the accumulation layer grows, which leads to a higher capacitance (C_{acc}). At moderate frequencies ($10\,\mathrm{Hz} < f < 1\,\mathrm{kHz}$), a stepwise increase of the capacitance can be observed which leads to a plateau formation in the capacitance characteristics. This phenomenon, which constitutes the core of this chapter, is further discussed starting from Section 4.3.

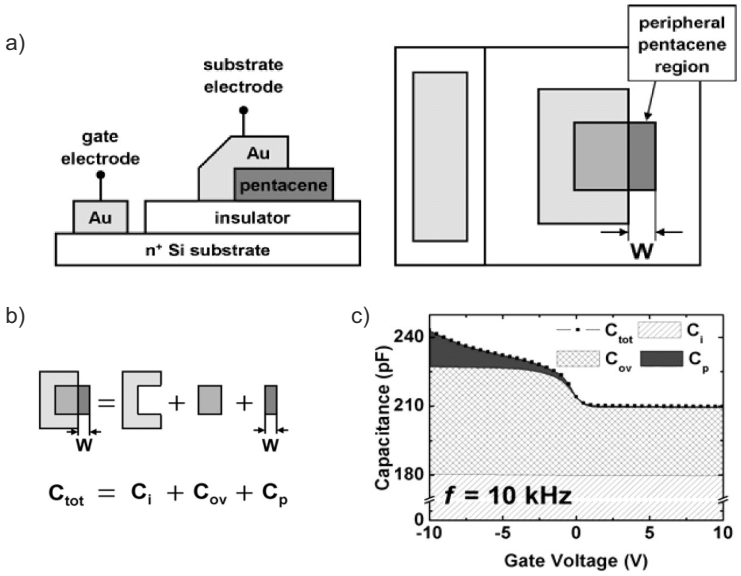

Figure 4.6. (a) Cross-sectional view (left) and top view (right) of the modified MOS capacitor structure. Peripheral pentacene region indicates the pentacene layer not covered by the gold electrode. (b) The overall capacitance is considered as the sum of three different capacitances in parallel, i.e. $C_{\mathrm{tot}} = C_{\mathrm{i}} + C_{\mathrm{ov}} + C_{\mathrm{p}}$. (c) The measured small-signal capacitance C_{tot} and the contribution of each partial capacitance. Reprinted from Ref. [201] © 2006 IEEE.

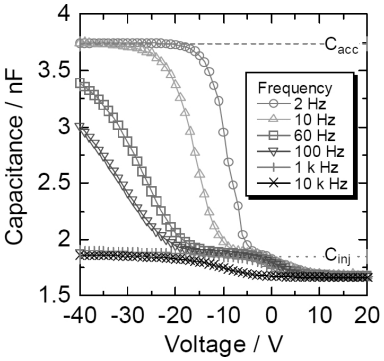

Figure 4.7. Small-signal C–V curves of a pentacene OTFT for frequencies from 2 Hz to 10 kHz. Bias is applied between the gate and source while the drain is electrically floating. Reprinted from Ref. [202] with permission from SPIE.

4.2 Experimental

C–V characterization is performed on two different MOS capacitor structures. The cross-section of the first type of MOS capacitor is given in Fig. 4.8. Devices are fabricated on highly doped Si^{++} wafers with 300 nm thermally grown oxide, which act as gate electrode and gate oxide, respectively. Oxide surface is wet cleaned with acetone, isopropanol and deionized water. In order to remove any organic contaminations, wafers are processed with an ozone cleaner. The organic semiconductor pentacene is purchased from Sigma-Aldrich and a 100 nm thin-film is thermally evaporated at 10^{-6} mbar through a shadow mask. Finally, a 20 nm gold (Au) layer is sputtered through the same shadow mask to finish the fabrication.

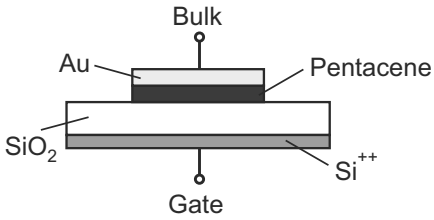

Figure 4.8. Cross-section of a fabricated MOS capacitor. Not to scale. Reprinted from Ref. [192] with permission from Elsevier.

As we mentioned in the previous section, investigations on the MOS capacitors, whose structure is given in Fig. 4.8 exclude the channel region of an OTFT, i.e. the semiconducting film between the source and drain electrodes. Therefore, by changing the shadow masks used in the last two fabrication steps, we prepared an alternative MOS capacitor structure (MOSCap), which resembles one half of an OTFT (Fig. 4.9b). *C–V* analysis performed on this structure takes into account the contribution of the channel region, i.e. the peripheral pentacene film extending beyond the Au electrode. Since a typical OTFT is laterally symmetric (symmetry axis is shown with the dashed line A–A′ in Fig. 4.9a), electrical analysis performed on a MOSCap can be easily interpreted to understand the *C–V* behavior of OTFTs.

C–V characterization is performed by using the QSCV mode of an Agilent precision semiconductor parameter analyzer (4156C). A bias (V_G) is applied to the gate electrode while the bulk electrode is connected to the ground. Measurements are performed in air where the devices are kept in the dark using a Süss

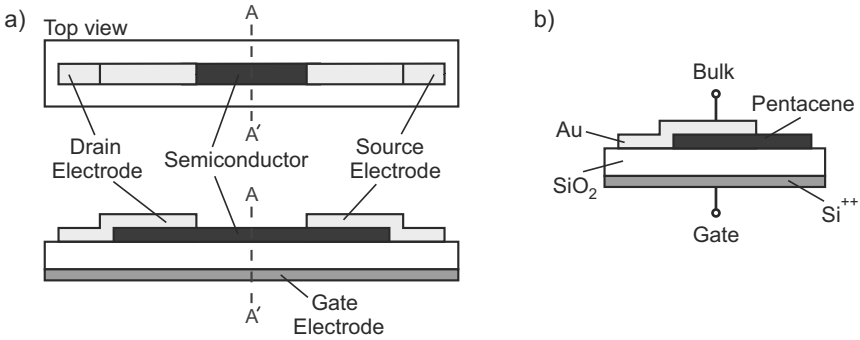

Figure 4.9. (a) Cross-section and top view of a bottom-gate staggered OTFT. Dashed line A–A′ shows the axis of lateral symmetry. (b) Cross-section of a MOSCap structure with peripheral pentacene which corresponds to the channel region of an OTFT. Figures are not to scale. Reprinted from Ref. [192] with permission from Elsevier.

Microtec probe station. Triaxial cables are utilized in order to eliminate any parasitic cable capacitance. Slow voltage sweep rates in the range of 100 mV/s are utilized to attain reproducible measurement results which fulfill quasi-static characterization requirements. Cyclic voltage sweeps symmetric with respect to 0 V (between 80 V and −80 V) are performed to prevent any nonsymmetric bias effects. The important measurement parameters are given in Appendix A.2.

4.3 QSCV Characteristics of MOSCaps

The measured QSCV curves of a MOS capacitor with pentacene as the organic semiconductor are given in Fig. 4.10. Since holes are the dominant charge carriers which can be injected into the pentacene from Au electrode, high capacitance values due to accumulation of injected charge carriers at the dielectric interface are measured at negative gate voltages ($V_G < 0$). Moreover, a clear hysteresis behavior with higher capacitance values during OFF-to-ON sweep, i.e. V_G towards more negative voltages, is observed. This is in accordance with the hysteresis in the transfer characteristics of OTFTs (higher I_{DS} during OFF-to-ON sweep) which we have presented in the previous chapter (Fig. 3.7). There, we have explained how the electronic trap states within the organic semiconductor can lead to hysteresis in the I–V characteristics of pentacene-based OTFTs by affecting the number of available charge carriers in the accumulation layer. Similarly, the hysteresis in the capacitance characteristics given in Fig. 4.10 can be

explained with the trapping of holes in the pentacene film as follows. At high positive gate voltages at the beginning of OFF-to-ON sweep, holes cannot be injected into the pentacene film, hence hole traps are empty and they have no effect on the capacitance. However, at negative gate voltages traps are filled with the increasing hole concentration at the dielectric interface. When the gate bias swings back to positive values (ON-to-OFF), trapped holes cannot react immediately, therefore, holes further away from the dielectric interface are forced to move instead. Thus, the distance between the gate electrode and the position of the holes which respond to gate bias changes increases and the capacitance drops below its value during OFF-to-ON sweep. Consequently, charge trapping in pentacene explains the hysteresis in the QSCV characteristics.

Another particular observation is the fact that the bias at which the measured capacitance departs from its minimum value during OFF-to-ON sweep is highly positive ($\sim$ 40 V). A similar characteristic has been reported by Lim *et al.* (Fig. 4.5b) where the authors suggest a mechanism of hole injection, which is assisted by trapped electrons within the semiconductor in the vicinity of Au source and drain electrodes.[180] According to this theory, the voltage at which the capacitance changes between its maximum and minimum values depends on the scan direction (Fig. 4.5). However, this is not the case for the results in Fig. 4.10, where no significant change in QSCV characteristics for different V_G scan directions is present. Therefore, we conclude that there must be another mechanism which is responsible for a C–V characteristics shift towards positive gate voltages. For example, negative oxide charges and interface states have been reported to cause similar effects in silicon MOS capacitors where holes are the majority charge carriers.[191] These effects are further investigated later in this section.

Figure 4.11 presents the measured QSCV characteristics of the MOSCap structure given in Fig. 4.9b. A similar hysteresis behavior as introduced above is observed. Nevertheless, different from the characteristics in Fig. 4.10, the QSCV characteristics of the MOSCap include a plateau similar to the small-signal C–V curves shown in Fig. 4.7. As we introduced in Section 4.1, Tanaka *et al.* related the plateau in the small-signal C–V characteristics with the slow spreading of charge carriers along the peripheral pentacene region.[202] However, this kind of transient effects can be ruled out for quasi-static measurements. Therefore, in the following we introduce another explanation for the plateau formation in the QSCV characteristics of MOSCaps.

In order to explain the plateau formation, the MOSCap structure is investi-

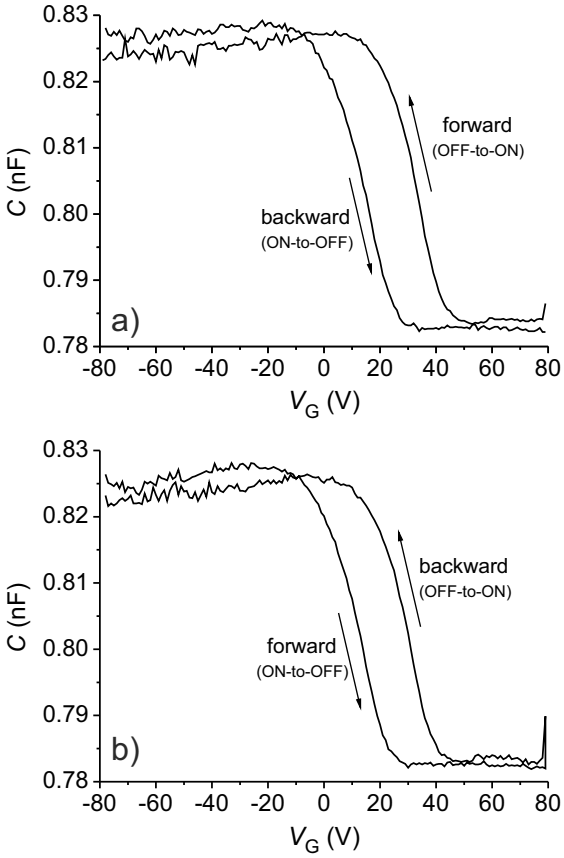

Figure 4.10. Measured QSCV characteristics of the MOS capacitor given in Fig. 4.8. V_G sweep direction is indicated by arrows. (a) Forward sweep is OFF-to-ON. (b) Forward sweep is ON-to-OFF. Reprinted from Ref. [192] with permission from Elsevier.

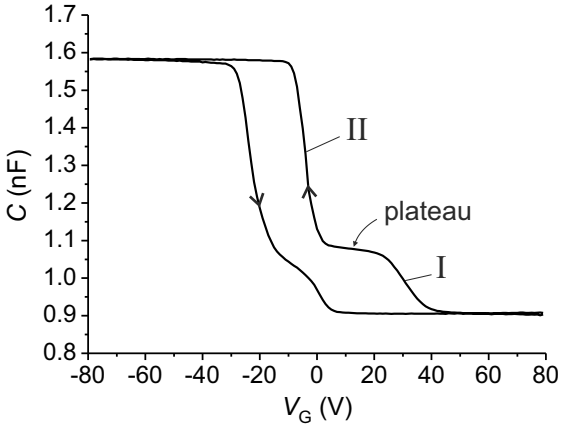

Figure 4.11. Measured QSCV characteristics of a MOSCap whose structure is given in Fig. 4.9b. Arrows indicate V_G sweep direction. Capacitance changes gradually in two steps which are marked with I and II for OFF-to-ON sweep. Reprinted from Ref. [192] with permission from Elsevier.

gated as a combination of three hypothetical parts, each with its individual C–V characteristics: (i) C_{ox} is the oxide capacitance due to the Au deposited on the gate oxide, (ii) C_{MOS} is the standard MOS capacitance of the sandwich structure made of Si^{++}, gate oxide, pentacene and Au, (iii) C_{peri} is the capacitance of the peripheral pentacene film which is not in contact with the Au electrode (Fig. 4.12). Since these partial capacitances are in parallel, as long as the fringing effects are neglected, the C–V characteristic of the overall structure (C_{MOSCap}) is equal to the sum of the individual characteristics of C_{ox}, C_{MOS} and C_{peri}.[201]

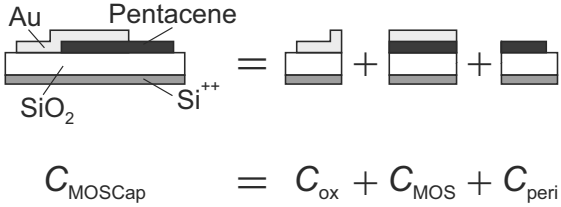

Figure 4.12. The MOSCap can be considered as a combination of three parts: Oxide capacitance C_{ox}, MOS capacitance C_{MOS}, and capacitance of the peripheral pentacene film C_{peri}. The capacitance of the overall structure (C_{MOSCap}) is equal to the sum of the capacitance of these parts. Reprinted from Ref. [192] with permission from Elsevier.

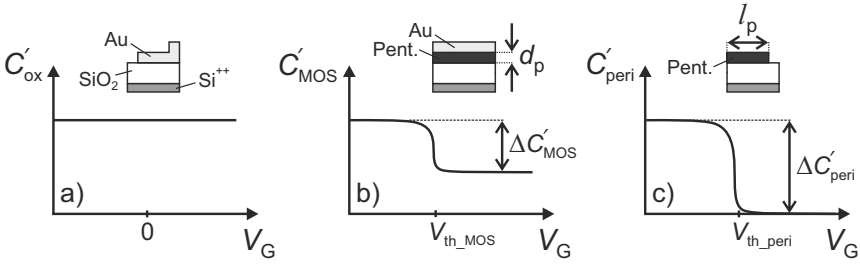

Figure 4.13. An illustration of the capacitance per unit area (C') versus gate voltage (V_{G}) characteristics of the partial capacitances given in Fig. 4.12. (a) Oxide capacitance C'_{ox}, (b) MOS capacitance C'_{MOS}, (c) capacitance of the peripheral pentacene film C'_{peri}, where d_{p} is the thickness of the pentacene film, l_{p} is the length of the peripheral pentacene film and V_{th} is the threshold voltage. Reprinted from Ref. [192] with permission from Elsevier.

Figure 4.13 presents an illustration of the C–V characteristics for the MOSCap parts introduced above. In order to exclude the geometrical dependencies normalized capacitances per unit area (C') are illustrated. The Au, which is deposited onto the SiO_2 forms a parallel plate capacitor whose capacitance is voltage independent as long as the depletion in the highly doped silicon (Si^{++}) gate is neglected. Therefore, C'_{ox} remains constant for any gate voltage (V_{G}) (Fig. 4.13a). C'_{MOS}, on the other hand, is voltage dependent as it has been explained in Section 4.1. Depending on the applied bias, C'_{MOS} changes between a maximum, which is equal to C'_{ox} when the charge carriers (holes) injected from Au electrode accumulate at the dielectric interface, and a minimum when the semiconductor film is depleted and only the charge carriers on the electrodes respond to the gate bias. The bias at which the capacitance starts to increase corresponds to the threshold voltage of of the MOS structure which is marked with $V_{\mathrm{th\_MOS}}$ in Fig. 4.13b. The last partial capacitance, C'_{peri}, also depends on the gate bias (Fig. 4.13c). Since charge carriers can be injected into and removed from the peripheral film through the adjacent pentacene layer, C'_{peri} increases to C'_{ox} when the film is in accumulation and decays to zero otherwise since there are not any charge carriers which can respond to the gate bias once the peripheral film is depleted. The voltage at which the charge injection into the peripheral film starts is marked with $V_{\mathrm{th\_peri}}$ which is not necessarily equal to $V_{\mathrm{th\_MOS}}$. Mechanisms which may cause $V_{\mathrm{th\_peri}}$ to differ from $V_{\mathrm{th\_MOS}}$ are discussed below.

In order to check the validity of the C–V characteristics illustrated in Fig.

4.13 and to determine how the C–V characteristics depend on the physical device dimensions, MOSCaps with different device geometries are investigated. In Figure 4.14 C–V characteristics of MOSCaps with various peripheral pentacene lengths (l_p) are given. The capacitance characteristics for $V_\mathrm{G} > 0$ are almost identical. Since C_peri is expected to decay to zero and thus not to contribute to the overall capacitance for $V_\mathrm{G} > V_\mathrm{th\_peri}$, it can be read from Fig. 4.14 that $V_\mathrm{th\_peri} \approx 0\,\mathrm{V}$ for our samples. For voltages less than $V_\mathrm{th\_peri}$, i.e. $V_\mathrm{G} < V_\mathrm{th\_peri}$, holes are injected into the peripheral pentacene film and the capacitance increases proportional to l_p. This characteristic can be observed in Fig. 4.14, where the change in the measured capacitance (ΔC_peri), which is marked with II, increases for longer l_p. Thus, considering the value of $V_\mathrm{th\_peri}$, we comment that the change in the capacitance marked with II in Fig. 4.11 is due to the contribution of C_peri to the overall capacitance.

In order to determine the contribution of C_MOS to the overall capacitance, further MOSCaps with various pentacene thicknesses (d_p) are investigated. Once again, C_MOS is expected to reach its maximum value for $V_\mathrm{G} < V_\mathrm{th\_MOS}$ when the injected charge carriers accumulate at the semiconductor-dielectric interface. Since the accumulation occurs always at the dielectric interface for the given MOSCap geometry, the maximum value of C_MOS is equal to C_ox which is independent of d_p. On the other hand, the minimum value of C_MOS, which is measured for $V_\mathrm{G} > V_\mathrm{th\_MOS}$, is inversely proportional to d_p as the separation of the Au and gate electrodes increases with increasing d_p. These characteristics can be observed in Fig. 4.15 where the maximum of the measured capacitance is constant–little fluctuations in the maximum capacitance value is in the range of shadow mask tolerances–while the minimum capacitance decreases with increasing d_p. Consequently, the change in C_MOS (ΔC_MOS) causes the transition marked with I in the measured characteristics. The voltage at which this transition starts refers to the threshold voltage of the MOS structure, which can be read as $V_\mathrm{th\_MOS} \approx 40\,\mathrm{V}$ from Fig. 4.15.

We have previously mentioned that $V_\mathrm{th\_MOS}$ and $V_\mathrm{th\_peri}$ are not necessarily the same. And the fact that $V_\mathrm{th\_MOS}$ is not equal to $V_\mathrm{th\_peri}$ is the reason why a plateau, which is shown in Fig. 4.11, exists in the C–V characteristics of a MOSCap. The well-known MOS theory predicts that traps, surface states and oxide charges lead to alterations in the C–V characteristics of a MOS capacitor by shifting or stretching out the curves along the voltage axis.[34] Therefore, in the following, we discuss whether any of these mechanisms can be related to

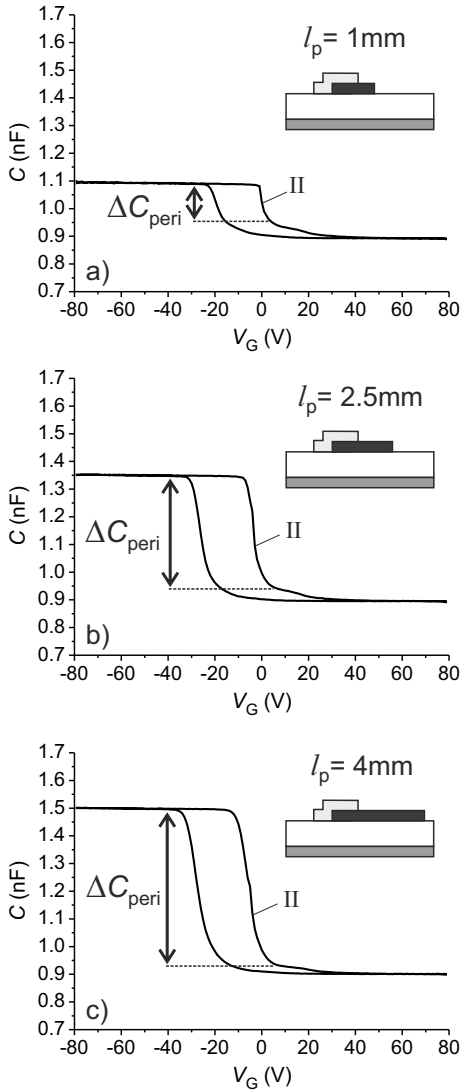

Figure 4.14. Measured C–V characteristics of MOSCaps with different peripheral pentacene film lengths (l_p). (a) $l_\mathrm{p} = 1\,\mathrm{mm}$, (b) $l_\mathrm{p} = 2.5\,\mathrm{mm}$, (c) $l_\mathrm{p} = 4\,\mathrm{mm}$. Pentacene film thickness $d_\mathrm{p} = 20\,\mathrm{nm}$. With increasing l_p, the maximum of the overall capacitance increases due to the increasing C_peri while the minimum capacitance is constant. Reprinted from Ref. [192] with permission from Elsevier.

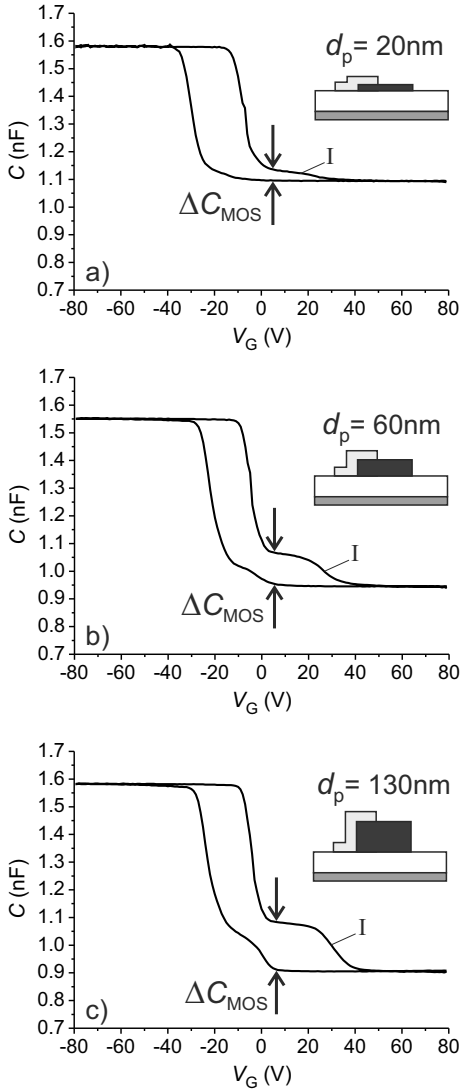

Figure 4.15. Measured C–V characteristics of MOSCaps with different pentacene film thicknesses (d_p). (a) $d_\mathrm{p} = 20\,\mathrm{nm}$, (b) $d_\mathrm{p} = 60\,\mathrm{nm}$, (c) $d_\mathrm{p} = 130\,\mathrm{nm}$. Peripheral pentacene film length $l_\mathrm{p} = 3\,\mathrm{mm}$. With increasing d_p, the minimum of the overall capacitance decreases due to the decreasing C_MOS while the maximum capacitance which is constant. The little fluctuation in the maximum capacitance value is probably caused by shadow mask tolerances. Reprinted from Ref. [192] with permission from Elsevier.

the formation of a plateau in the measured C–V curves. Since we are looking for an effect which influences $V_{\mathrm{th\_MOS}}$ and $V_{\mathrm{th\_peri}}$ differently, any mechanism that affects C_{MOS} and C_{peri} similarly can be ruled out. Thus, fixed, trapped or mobile ionic charges, which are distributed rather uniformly throughout the gate oxide or the semiconductor film, can be neglected and we concentrate our focus on the Au-pentacene interface, which exists only for the MOS section of the MOSCap structure. The already mentioned results from Lim *et al.* suggest that electron traps in the vicinity of Au electrode within the pentacene cause a shift in $V_{\mathrm{th\_MOS}}$.[180] However, this would require the C–V characteristics to be dependent on the gate bias sweep direction (see Fig. 4.5), which is not the case for our MOS samples as we have shown before (Fig. 4.10). Since the shift in $V_{\mathrm{th\_MOS}}$ is towards positive gate bias and it is independent of the bias sweep direction, we propose that negative fixed charges within or at the surface of the pentacene film cause the shift. Previous studies have reported that metals penetrate into the organic films onto which they are deposited and generate various charge states within these films.[203–205] Sawabe *et al.* demonstrated that Au atoms penetrate polycrystalline pentacene films up to a depth of about 150 nm.[206] Therefore, it is very probable that the shift of $V_{\mathrm{th\_MOS}}$ is due to the charge states at the pentacene-SiO_2 interface, which are caused by Au deposition.[207] These states would only affect $V_{\mathrm{th\_MOS}}$ as no Au is deposited onto the peripheral pentacene film. In order to verify this theory, we calculate the surface charge carrier density (Q_{sc}) which is necessary to cause a threshold voltage shift (ΔV_{th}) of about 40 V according to

$$\Delta V_{\mathrm{th}} = -\frac{Q_{\mathrm{sc}}}{C_{\mathrm{i}}}, \tag{4.3}$$

where C_{i} is the capacitance of the insulator.[34] The calculated surface charge carrier density of $2.87 \times 10^{12}\,\mathrm{cm}^{-2}$ is in the order of the surface charge densities reported in the literature.[208, 209]

4.4 Simulations

In order to investigate the effects of charge traps in the semiconductor and surface charges at the dielectric interface on the capacitance characteristics of organic MOS capacitors, we perform numerical simulations with the physical device simulator ATLAS (Silvaco). Simulations are performed for device structures

given in Figs. 4.8 and 4.9b. Material parameters for pentacene are set identical to the values given in Section 3.4. In order to simulate the capacitance, a constant voltage ramp (dV/dt) is used where the displacement current (I_{dis}) is monitored. Since dV/dt is constant, in accordance with (2.7), the capacitance can be easily read from

$$C = \frac{I_{\mathrm{dis}}}{dV/dt}. \tag{4.4}$$

Figure 4.16 shows the simulated C–V characteristics for a MOS capacitor without peripheral pentacene film for a trap density of $2 \times 10^{19}\,\mathrm{cm}^{-3}$ at a discrete energy level of 0.1 eV above the HOMO band of pentacene and trap lifetimes of 5 s and 140 s. Results show that the presence of traps causes a hysteresis in C–V characteristics.

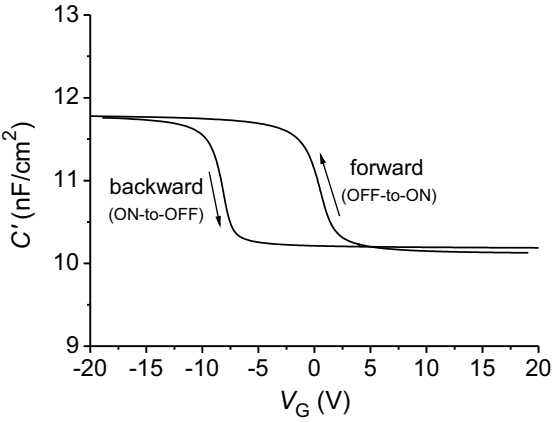

Figure 4.16. Simulation of the capacitance per unit area (C') versus gate voltage (V_{G}) characteristics of the MOS capacitance given in Fig. 4.8 with a trap density of $2 \times 10^{19}\,\mathrm{cm}^{-3}$ in the organic semiconductor.

In order to investigate the role of surface charges on the capacitance behavior, we perform further simulations where the previously calculated surface charge carrier density of $2.87 \times 10^{12}\,\mathrm{cm}^{-2}$ is introduced. This time a MOSCap structure (see Fig. 4.9b) with peripheral pentacene region is used for the simulation. Results given in Fig. 4.17 show that surface charges cause a shift in $V_{\mathrm{th\_MOS}}$ which leads to C–V characteristics with a plateau.

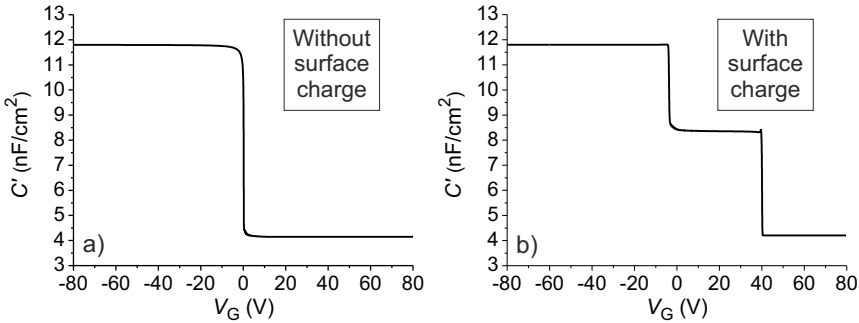

Figure 4.17. Simulation of the capacitance per unit area (C') versus gate voltage (V_{G}) characteristics of the MOSCap given in Fig. 4.9b. (a) Without surface charges. (b) With surface charges with a density of $2.87 \times 10^{12}\,\mathrm{cm}^{-2}$.

Thus, the above given simulation results support the theory, which we introduced in the previous section to explain the hysteresis and the plateau formation in measured QSCV characteristics.

4.5 Behavioral Modeling

Understandings of the previous sections are utilized to implement a behavioral PSpice model for MOSCaps. In accordance with Fig. 4.12, the model basically consists of three tunable capacitances (C_{ox}, C_{MOS}, C_{peri}) in parallel where each capacitance can be dimensioned according to the actual geometry of the device to be simulated (Fig. 4.18). C_{ox} is voltage-independent, therefore, it can be implemented with a standard capacitor in PSpice. Yet, C_{MOS} and C_{peri} are voltage-dependent nonlinear capacitances which are not found in standard PSpice libraries. In order to implement a voltage-dependent nonlinear capacitance we employ a voltage-controlled current-source (VCCS) as shown in Fig. 4.19, where the current is set to be proportional to the derivative of the voltage as in accordance with (4.4) so that

$$I(V) = \frac{dQ(V)}{dt} = C(V)\frac{dV}{dt}. \tag{4.5}$$

In order to reproduce the nonlinear capacitance behavior, a hyperbolic tangent function is used to define the voltage dependence of the capacitance as

$$C(V) = k_{\mathrm{a}}\tanh(k_{\mathrm{s}}V + k_{\mathrm{x}}) + k_{\mathrm{y}}. \tag{4.6}$$

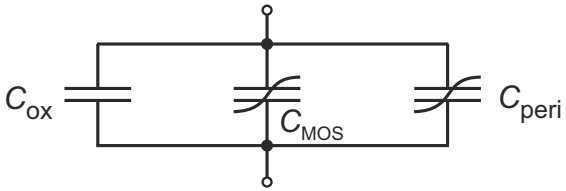

Figure 4.18. Block diagram of the behavioral model for the QSCV characteristics of a MOSCap. Reprinted from Ref. [192] with permission from Elsevier.

As illustrated in Fig. 4.20, the model parameters k_a, k_s, k_x, and k_y in (4.6) determine the amplitude, slope, x-axis offset and y-axis offset of the modeled characteristics, respectively. Parameters k_a and k_y set together the minimum and maximum values of the capacitance. Therefore, they primarily depend on the device geometry, i.e. the area of the contacts (A), the thickness of the dielectric (d), and the relative permittivity of the insulating layer (ε_r), according to (4.2). The parameter k_x introduces an offset along the voltage axis, thus it can be used to fit the threshold voltage of the characteristics. And, finally, the parameter k_s defines the slope of the characteristics between maximum and minimum capacitance values, which corresponds to the change between charge accumulation and charge depletion within the organic semiconductor.

Figure 4.21 shows the behavioral model for the C–V characteristics of a MOSCap. In addition to the circuit given in Fig. 4.18, the model contains an auxiliary RC network which is utilized to implement the hysteresis behavior as we have explained in Section 3.5.[145] The voltage across the capacitance (V_{RC}) in each branch of the RC network is used as a variable to shift the capacitance char-

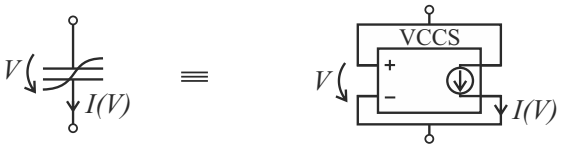

Figure 4.19. Nonlinear voltage-dependent capacitor behavior is modeled with a voltage-controlled current-source (VCCS) in PSpice. A hyperbolic tangent function is used to model the nonlinear voltage dependence of the capacitance. k_a, k_s, k_x, and k_y are constants which are used as fitting parameters. Reprinted from Ref. [192] with permission from Elsevier.

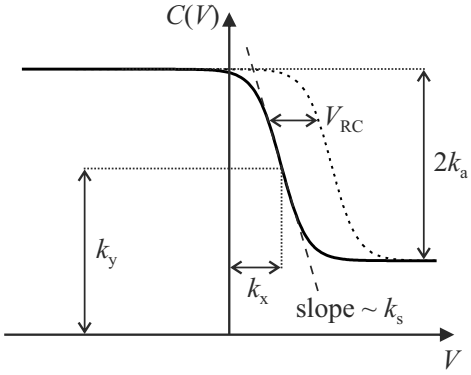

Figure 4.20. The dependency of the modeled nonlinear voltage-dependent capacitance characteristics on model parameters. The parameter k_a, k_s, k_x, and k_y in (4.6) determine the amplitude, slope, x-axis offset, and y-axis offset of the characteristics, respectively. The variable V_RC is utilized to reproduce the hysteresis behavior. Reprinted from Ref. [192] with permission from Elsevier.

acteristics along the voltage axis in order to reproduce the hysteresis behavior (Fig. 4.20). Inserting V_RC into (4.6) results in

$$C_\mathrm{MOS}(V) = k_\mathrm{a1}\tanh(k_\mathrm{s1}V + k_\mathrm{x1} + V_\mathrm{RC\_MOS}) + k_\mathrm{y1}, \tag{4.7}$$

$$C_\mathrm{peri}(V) = k_\mathrm{a2}\tanh(k_\mathrm{s2}V + k_\mathrm{x2} + V_\mathrm{RC\_peri}) + k_\mathrm{y2}, \tag{4.8}$$

where $V_\mathrm{RC\_MOS}$ and $V_\mathrm{RC\_peri}$ are the voltages across the capacitances in different branches of the RC network (Fig. 4.21). The auxiliary RC network is decoupled from the rest of the model with a unity gain voltage-controlled voltage-source (VCVS). Further information on PSpice model parameters is given in Appendix B.2. A comparison between the measured and the simulated QSCV characteristics in Fig. 4.22 validates the introduced behavioral model.

4.6 Conclusions

In this chapter we have presented the quasi-static C–V (QSCV) characteristics of organic capacitor structures. In addition to standard MOS capacitors, capacitor structures with a peripheral pentacene layer (MOSCaps) are fabricated in order to investigate the influence of the channel region of an OTFT in the QSCV analysis. Independent of the device structure, a hysteresis is observed in the QSCV

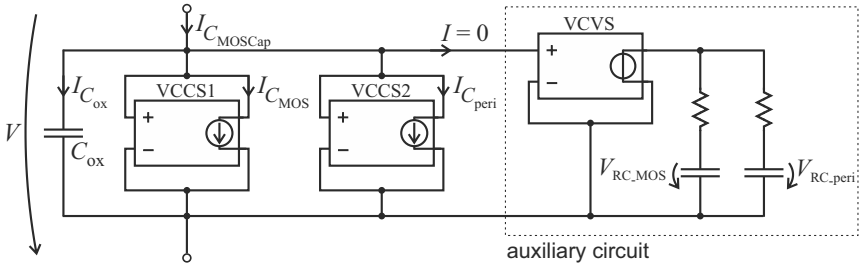

Figure 4.21. PSpice behavioral model for the QSCV characteristics of a MOSCap. The constant oxide capacitance C_{ox} is modeled with a standard capacitor while the nonlinear capacitances C_{MOS} and C_{peri} are each implemented with a VCCS according to (4.7) and (4.8), respectively. The model includes an auxiliary RC network which is utilized to implement the hysteresis behavior. Reprinted from Ref. [192] with permission from Elsevier.

curves which can be explained with the charge carrier trapping in the organic semiconductor. On the other hand, the QSCV characteristics of MOSCaps include a plateau which can be related to surface states caused by Au diffusion into pentacene during top electrode deposition. This has been investigated by fabricating MOSCaps with different pentacene film thicknesses and peripheral pentacene lengths. A surface charge carrier density of $2.87 \times 10^{12}\,\mathrm{cm}^{-2}$ is calculated which is in the order of the densities reported in the literature for similar device structures.

The hysteresis and the plateau in the QSCV characteristics have been further investigated through device simulations with ATLAS. Simulation results confirm that majority carrier trapping leads to the hysteresis in the QSCV curves just like the hysteresis in I–V curves, which we have studied in the previous chapter. Moreover, it has been shown that introducing surface charges leads to a plateau formation in the QSCV curves. Consequently, through measurements and simulations we have shown how the overall capacitance behavior depends on different sections of a MOSCap.

These understandings are then utilized to introduce a PSpice behavioral model which allows the QSCV characteristics of MOSCaps to be simulated. For this purpose, the nonlinear capacitance characteristics are modeled with voltage-controlled current-sources while an RC network is introduced to reproduce the hysteresis behavior. An important advantage of the model is its capability to be adapted for various device geometries and dimensions, such that it can be employed to predict QSCV characteristics of devices prior to fabrication.

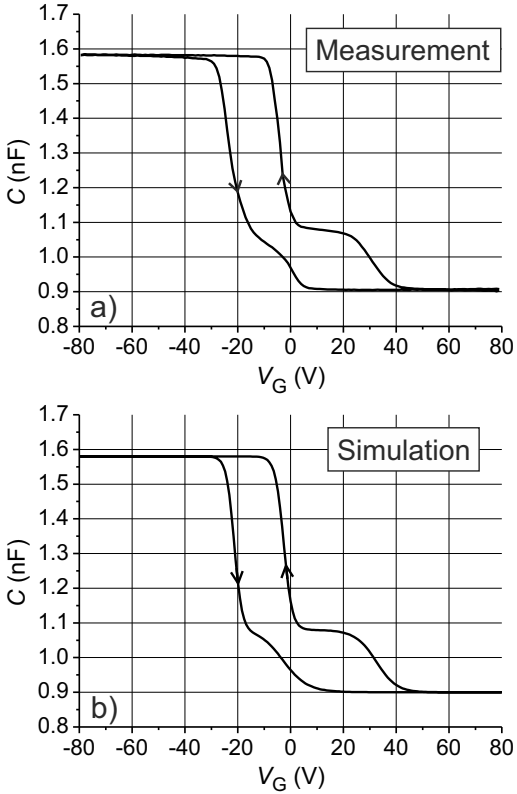

Figure 4.22. (a) Measured QSCV characteristics of a MOSCap. (b) QSCV characteristics of a MOSCap is simulated in PSpice with the behavioral model given in Fig. 4.21. Reprinted from Ref. [192] with permission from Elsevier.

Chapter 5

Conclusions and Outlook

Transient and bias dependent instabilities in the current-voltage (I–V) and capacitance-voltage (C–V) characteristics of pentacene-based organic thin-film transistors (OTFTs) are investigated in this thesis. Through measurements and device simulations, we have shown that trapping of majority charge carriers, i.e. holes, in the organic semiconductor pentacene can satisfactorily explain the hysteresis observed in the I–V and C–V characteristics. Furthermore, we have developed behavioral PSpice models, which can reproduce the electrical device characteristics of OTFTs.

In Chapter 3, the I–V characteristics of OTFTs are studied. Hole trapping induced hysteresis is observed both in output and transfer characteristics. From transient measurements, we have extracted trapping time constants as $\tau_1 = 5\,\mathrm{s}$, $\tau_2 = 140\,\mathrm{s}$ and the area density of traps as $\sigma_t = 2 \times 10^{11}\,\mathrm{cm}^{-2}$. Through device simulations with ATLAS, it is verified that these trap states in the organic semiconductor can lead to a hysteresis in the I–V characteristics. With the help of transfer characteristics, it is shown that the above mentioned hysteresis can be modeled with a threshold voltage shift. We have utilized this approach to develop a behavioral OTFT model in PSpice, which can successfully reproduce both sweep and transient characteristics including hysteresis effects.

Due to long time constants of trapping dynamics, which require longer time to settle compared to the duration of standard electrical measurements, identical measurements performed subsequently on the same device can lead to diverse results. In order to eliminate this, we have introduced an initialization routine to be performed prior to measurements, which is shown to increase the repro-

ducibility and reliability of measurement results. Yet, in sweep measurements such as output and transfer characteristics measurements, despite initialization routines, the prolonged effects of a bias applied at the beginning of the measurement can modify the device response in later stages of the same measurement. We have presented that this can lead to a change in the width and even in the rotational direction of the observed hysteresis. Therefore, we suggest, it shall be a routine to comment on the electrical measurement parameters such as hold time, delay time, and voltage sweep rate in all studies concerning OTFTs since the electrical measurement parameters may have a profound influence on the measured device characteristics.

The quasi-static C–V (QSCV) characteristics of organic metal-oxide-semiconductor (MOS) structures are investigated in Chapter 4. In addition to the MOS capacitor structure, which has been commonly used in the literature, an alternative MOS capacitor structure (MOSCap) with a peripheral pentacene layer is also studied. The advantage of the latter is the fact that it perfectly resembles one half of an OTFT, such that analyses performed on MOSCaps can be easily interpreted to understand the QSCV characteristics of OTFTs.

We have shown, independent of the capacitor structure, a hysteresis exists in the QSCV characteristics, which can also be explained with charge trapping within the organic semiconductor. However, more interestingly, a plateau is observed in the QSCV characteristics of MOSCaps, which, to our knowledge, has not been previously reported in the literature. We have proposed, surface states with a density of $2.87 \times 10^{12}\,\mathrm{cm}^{-2}$, which stem from Au diffusion into pentacene during device fabrication, lead to the plateau formation in the QSCV curves. This explanation is verified through device simulations with ATLAS, which have also demonstrated the relationship between charge trapping in the organic semiconductor and the hysteresis in the QSCV characteristics. Last but not least, a behavioral PSpice model is introduced, which can reproduce the measured QSCV characteristics of organic MOS structures. This model allows the QSCV characteristics of OTFTs with various device geometries and dimensions to be studied prior to fabrication.

Finally, we would like to suggest several directions of possible studies, which, we think, can benefit from the results presented in this thesis. Apart from memory applications, hysteresis is an undesirable effect for standard integrated circuits. Therefore, two opposite approaches can be followed in future studies. The first approach would be enhancing the hysteresis in order to realize a bistable

memory functionality, whereas the other approach would be eliminating the hysteresis in order to increase the stability of circuits with OTFTs. We have shown in this thesis that the hysteresis is proportional to the ratio of density of trap states to the density of free charge carriers in the active layer of an OTFT. Therefore, substituting pentacene with other organic semiconductors should be expected to change the trap density and the resulting hysteresis. On the other hand, since the trap density is not only determined by the choice of material but also depends on the fabrication methods and environmental conditions, which affects, for example, the quality and structural ordering of the resulting films, the density of impurity atoms, and the unintentional doping, these can also be utilized to tailor the hysteresis.

One of the most important prerequisites for realization of more complex OTFT circuitry, is the availability of accurate device models, which can be utilized in circuit simulations. With the behavioral models introduced in this thesis, we have contributed to the efforts to develop a compact OTFT model. Yet, a complete model does not exist at the moment. Therefore, another interesting future work would be to develop a compact device model, which can reproduce both the static and dynamic electrical characteristics of OTFTs.

Appendix A

Measurement Parameters

A.1 Current-Voltage (I–V) Characterization

	V_{DS}				V_{GS}					
	Start	Stop	Step	Sweep mode†	Start	Stop	Step	Sweep mode†	t_{hold}	t_{delay}
Fig. 3.7	−80 V	−80 V	-	-	20 V	−80 V	−5 V	cyclic	3 s	10 ms
Fig. 3.10a	20 V	−80 V	−5 V	cyclic	0 V	−80 V	−20 V	*single*	3 s	10 ms
Fig. 3.10b	20 V	−80 V	−5 V	cyclic	−80 V	0 V	20 V	*single*	3 s	10 ms
Fig. 3.18a	20 V	−80 V	−5 V	cyclic	20 V	−80 V	−20 V	*single*	10 s	3 s
Fig. 3.18b	20 V	−80 V	−20 V	*single*	20 V	−80 V	−5 V	cyclic	10 s	3 s
Fig. 3.21a	0 V	−80 V	−5 V	cyclic	−80 V	−80 V	-	-	30 s	1 s
Fig. 3.21b	0 V	−80 V	−5 V	cyclic	−80 V	−80 V	-	-	3 s	1 s
Fig. 3.21c	0 V	−80 V	−5 V	cyclic	−80 V	−80 V	-	-	0 s	1 s

†For measurements where more than one parameter are swept consecutively, the sweep mode of the secondary sweep parameter (see Fig. 2.19) is given in *italics*.

A.2 Capacitance-Voltage (C–V) Characterization

	V_G							
	Start	Stop	Step	Sweep mode	ΔV[†]	Δt[†]	t_{hold}[‡]	t_{delay}[‡]
Fig. 4.10	80 V	−80 V	−1 V	cyclic	0.1 V	1 s	100 s	10 s
Fig. 4.11	80 V	−80 V	−1 V	cyclic	1 V	1 s	100 s	10 s
Fig. 4.14	80 V	−80 V	−1 V	cyclic	1 V	1 s	100 s	10 s
Fig. 4.15	80 V	−80 V	−1 V	cyclic	1 V	1 s	100 s	10 s

[†] $\Delta V/\Delta t$ determines the ramp rate of the quasi-static measurement (see Fig. 2.20b).

[‡] Please refer to Agilent 4155C/4156C Semiconductor Parameter Analyzer–User's Guide[210] for further information on timing issues of measurements.

Appendix B

Modeling Parameters

B.1 Behavioral Current-Voltage (I–V) Model Parameters

Please refer to Fig. 3.17 for parameters given below.

τ_1		τ_2		c_1	c_2	f_{PWL}
5 s		140 s		0.15	0.85	see Fig. B.1
$C = 50\,\mu F$	$R = 100\,k\Omega$	$C = 1.4\,mF$	$R = 100\,k\Omega$			

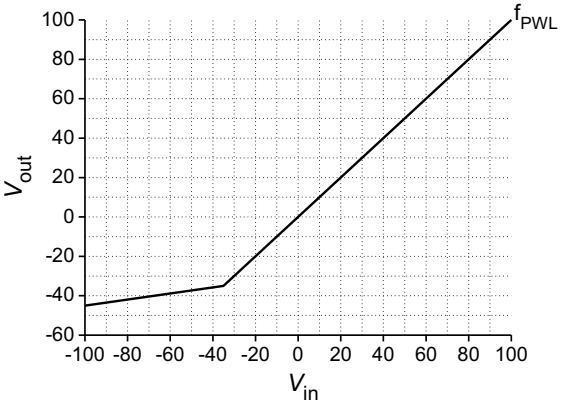

Figure B.1. Piecewise linear function (f_{PWL}), which is depicted in Fig. 3.17, is used to compensate different V_{th} dependency of I_{DS} in linear and saturation regimes.

B.2 Behavioral Capacitance-Voltage (C–V) Model Parameters

Please refer to Eqs. (4.7) and (4.8) and Fig. 4.21 for parameters given below.

C_{ox}	440 pF	
C_{MOS}	k_{a1}	90 pF
	k_{s1}	−0.12
	k_{x1}	−12 V
	k_{y1}	550 pF
C_{peri}	k_{a2}	250 pF
	k_{s2}	−0.33
	k_{x2}	13 V
	k_{y2}	250 pF
$\tau_{\mathrm{RC\_MOS}}$ †	C	100 µF
	R	100 kΩ
$\tau_{\mathrm{RC\_peri}}$ ‡	C	200 µF
	R	100 kΩ

† Values refer to the left branch of the RC network in the auxiliary circuit in Fig. 4.21, which sets $V_{\mathrm{RC\_MOS}}$.

‡ Values refer to the right branch of the RC network in the auxiliary circuit in Fig. 4.21, which sets $V_{\mathrm{RC\_peri}}$.

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Publication List

Publications in journals

1. F. A. Yildirim, **C. Ucurum**, R. R. Schliewe, W. Bauhofer, R. M. Meixner, H. Goebel, and W. Krautschneider, *Spin–cast composite gate insulation for low driving voltages and memory effect in organic field–effect transistors*, Appl. Phys. Lett. 90(8) 083501 (2007).

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1. **C. Ucurum**, H. Goebel, *Investigation on parasitic capacitance effects in organic thin–film transistors*, International Conference on Organic Electronics, ICOE 2011, Rome, Italy (2011).

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